

1 Features

- 4 Majority Gate Interfaces
 - MGI00, MGI01, MGI02 and MGI03 are all fed through the PLL
- Each MGI is comprised of:
 - One D2P block, to excite the SW MAJ inputs
 - One P2D block, to interpret the SW MAJ output
- Fractional-N PLL at 5.92 – 6.9GHz
- Phase inversion control per D2P antenna driver
- D2P maximum output power: 0dBm at 50Ω, gain control range: 30dB
- P2D conversion gain control range: 12dB
- Phase Shifter with digital controls
- 4-wire Serial Peripheral Interface (SPI) control
- 33 static registers
- 10bit ADC
- Power detection in each D2P output (12 total)
- CMOS MAJ for validation of SW MAJ
- Extensive Analog Test Bus (ATB)
- Controllable PLL, MGI and ADC bias currents
- Controllable LDO Voltages
- 4-bit chip address
- Supply voltage 1.8V, different domains for each MGI
- Size: $3.23 \times 3.23\text{mm}^2$

2 General Description

SPIDER APIC 2 is a CMOS Integrated Circuit (IC), which enables information transferring between the CMOS circuitry and the Spinwave Majority Gates (SW MAJ). It consists of 4 Majority Gate Interfaces (MGI), each one capable of exciting properly a SW MAJ and also interpreting the SW MAJ produced output. A Phased-Locked Loop (PL312) is used to feed the MGIs with the necessary RF reference signal, in order to avoid the more complex RF routing in the interposer level. A 4-wire SPI is used to digitally control the IC's internal circuitry, allowing the user to exploit the various available features and functionalities.

The die size is $3.23 \times 3.23\text{mm}^2$ and has been packaged in a 236-ball chip scale package (CSP), with a pitch of $160\mu\text{m}$.

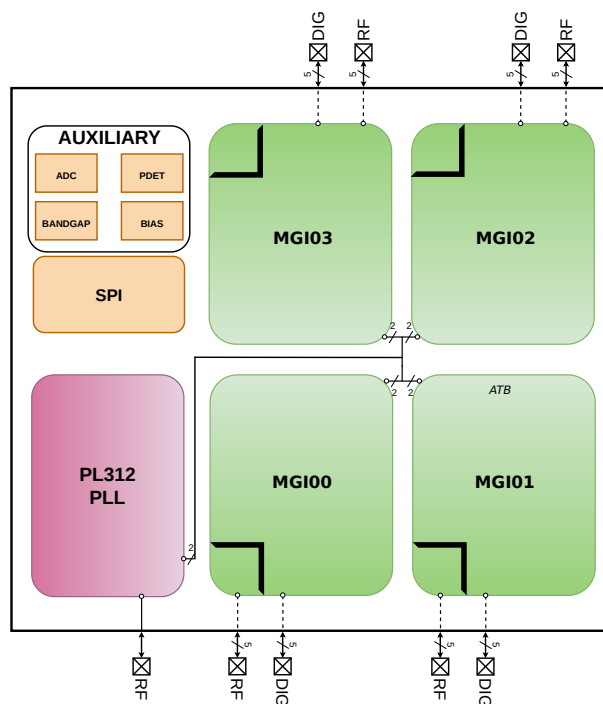


Figure 1: Simplified block diagram.

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3 Revision History

3.1 Revision 1.0

Date	Section Number	Description
07/09/2026	-	Initial release

4 Functional Block Diagram

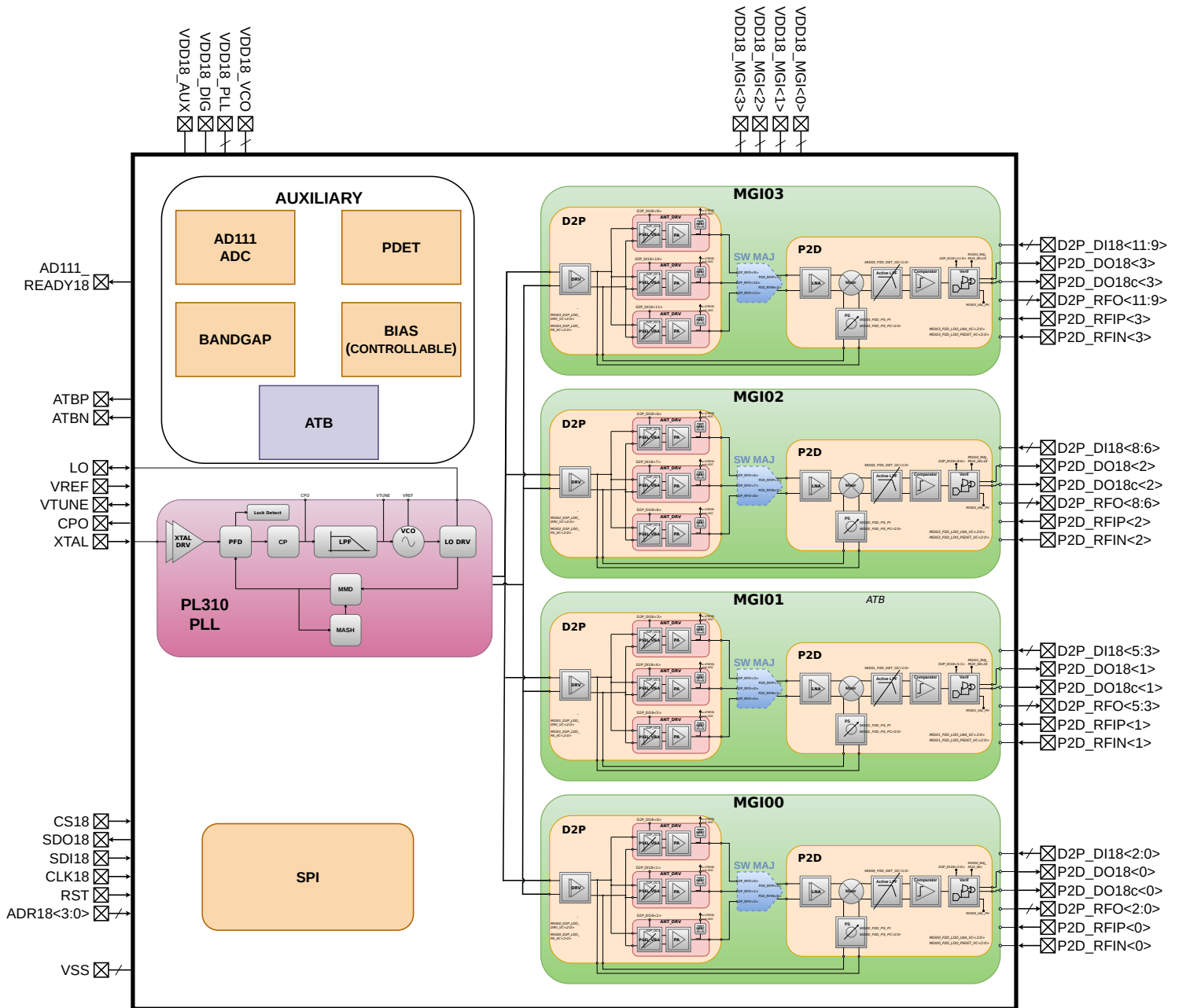


Figure 2: Functional block diagram.

5 Supply Current and Power Consumption Specifications

Parameter	Min.	Typ.	Max.	Unit	Comment
Supply Characteristics					
VDD18_* pins	1.7	1.8	1.9	V	
Positive Supply Current					DC steady state operation
APIC 1		474.66		mA	4*MGI + PLL + SPI + AUX
MGI		96.04		mA	
D2P		61.8		mA	
P2D		34.24		mA	
PLL (PL312)		75		mA	When LO pin is not used
SPI		4.7		mA	
AUX		10.8		mA	
Power Down Positive Supply Current					DC steady state operation
APIC 1		7.3		mA	SPI + AUX
MGI		3		uA	
D2P		2.6		nA	
P2D		465		nA	
PLL (PL310)		2.9		μA	
AUX		2.6		mA	
MGI Power Consumption					
D2P		111.24		mW	
P2D		61.63		mW	

Table 1: Current and power consumption specifications.

6 Typical Specifications

Parameter	Min	Typ	Max	Unit	Comments
D2P					
Frequency of interest		6.5		GHz	
Maximum Gain		12		dB	At 6.5GHz
Gain Temperature Variation	-2.6		+2.3	dB	At 6.5GHz
Maximum Output Power		0		dBm	At 6.5GHz
Gain Control Range	25	30		dB	
Gain Control Step	0.5	1		dB	
Phase Inversion		180		deg	
Output Return Loss		-6.28		dB	At 6.5GHz
Output Impedance		50		Ω	Single-Ended
P2D					
Frequency of interest		6.5		GHz	
Maximum Conversion Gain		38		dB	
Conversion Gain Control Range		12		dB	
Conversion Gain Control Step		2 to 7		dB	
Minimum Detectable Input Signal		-42		dBm	
Phase Shifter Range		>360		deg	
Phase Shift Step	35	45	60	deg	Over PVT
Integrated Noise Figure		26		dB	Measured at LPF output
Nominal 1dB LNA Input Comp. Point		-35		dBm	
Input Return Loss		-13.8		dB	At 6.5GHz
Input Impedance		70		Ω	Differential

Table 2: Typical specifications.

7 Pin Configuration & Description

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A		VSS	ATBN	ATBP	VDD18_AUX	VDD18_MGI<3>	P2D_DO18<3>	P2D_DO18<3>	D2P_DI1<8>	D2P_DI1<8>	D2P_DI1<8>	VSS	D2P_DI1<8>	D2P_DI1<8>	D2P_DI1<8>	P2D_DO18<2>	P2D_DO18<2>	VDD18_MGI<2>	VSS	
B	VSS	VSS				VDD18_MGI<3>	VDD18_MGI<3>	VDD18_MGI<3>	VDD18_MGI<3>	VDD18_MGI<3>	VSS	VDD18_MGI<2>	VDD18_MGI<2>	VDD18_MGI<2>	VDD18_MGI<2>	VDD18_MGI<2>	VDD18_MGI<2>	VDD18_MGI<2>	VSS	VSS
C	VSS					VSS	VSS	VSS		VSS		VSS	VSS	VSS	VSS		VSS			VSS
D	VSS						VSS		VSS	P2D_RFIN<3>	VSS	VSS		VSS		VSS	P2D_RFIN<2>	VSS		VSS
E	VSS					VSS	D2P_RFO<11>	VSS	VSS	P2D_RFIP<3>	VSS	VSS	VSS	D2P_RFO<8>	VSS	VSS	P2D_RFIP<2>	VSS		CS18
F	AD111_READY18						VSS			VSS		VSS		VSS			VSS			SD018
G							VSS			VSS		VSS		VSS			VSS			SD118
H		VREF	VSS	LO	VSS	VSS	D2P_RFO<10>	VSS	VSS	D2P_RFO<9>	VSS	VSS	VSS	D2P_RFO<7>	VSS	VSS	D2P_RFO<6>	VSS		CLK18
I			VSS				VSS			VSS		VSS		VSS			VSS			VSS
J			VSS																	VDD18_DIG
K																				VSS
L	VTUNE		VSS				VSS			VSS		VSS		VSS			VSS			
M	VSS	VSS	VDD18_VCO	VSS		VSS	D2P_RFO<1>	VSS	VSS	D2P_RFO<0>	VSS	VSS	VSS	D2P_RFO<4>	VSS	VSS	D2P_RFO<3>	VSS		
N	VDD18_VCO	VDD18_VCO	VDD18_VCO	VSS			VSS			VSS		VSS		VSS			VSS			RSTB
O	VDD18_PLL	VDD18_PLL	VDD18_PLL	VDD18_PLL			VSS			VSS		VSS		VSS			VSS			AFB<0>
P	VSS		VSS	VDD18_PLL		VSS	D2P_RFO<2>	VSS	VSS	P2D_RFIP<0>	VSS	VSS	VSS	D2P_RFO<5>	VSS	VSS	P2D_RFIP<1>	VSS		ADR18<1>
Q	VSS	VSS		VSS			VSS		VSS	P2D_RFIN<0>	VSS	VSS		VSS		VSS	P2D_RFIN<1>	VSS		ADR18<2>
R	VSS	VSS	VSS	VSS		VSS	VSS	VSS		VSS		VSS	VSS	VSS	VSS		VSS			ADR18<3>
S	VSS	VSS		CPO		VDD18_MGI<0>	VDD18_MGI<0>	VDD18_MGI<0>	VDD18_MGI<0>	VDD18_MGI<0>	VDD18_MGI<0>	VSS	VDD18_MGI<1>	VDD18_MGI<1>	VDD18_MGI<1>	VDD18_MGI<1>	VDD18_MGI<1>	VDD18_MGI<1>	VSS	VSS
T		VSS	XTAL	VSS		VDD18_MGI<0>	P2D_DO18<0>	P2D_DO18<0>	D2P_DI1<8>	D2P_DI1<8>	D2P_DI1<8>	VSS	D2P_DI1<8>	D2P_DI1<8>	D2P_DI1<8>	P2D_DO18<1>	P2D_DO18<1>	VDD18_MGI<1>	VSS	

DC Power

Analog/RF I/O

Digital I/O

Ground

MGI

SPIDER APIC-2 BOTTOM VIEW

Figure 3: Pin configuration (IC BOTTOM VIEW).

Pin Name	Pin No.	Type	Description	Comments
VSS	A[2,12,19], B[1,2,12,19,20], C[1,6,7,8,10,12,13,14,15,17,20], D[1,7,9,11,12,14,16,18,20], E[1,6,8,9,11,12,13,15,16,18], F[7,8,10,12,14,17,18,20], G[7,10,12,14,17], H[3,5,6,7,8,9,11,12,13,15,16,18], I[3,7,10,12,14,17,20], J[3], K[20], L[3,7,10,14,17], M[1,2,4,6,8,9,11,12,13,15,16,17,18], N[4,7,10,12,14,17], O[7,10,12,14,17], P[1,3,6,8,9,11,12,13,15,16,17,18], Q[1,2,4,7,9,11,12,14,16,18], R[1,2,3,4,6,7,8,10,12,13,14,15,18], S[1,2,12,19,20] T[2,4,12,19]	Supply	Ground	Connect to groundplane
VDD18_MGI <0>	S6, S7, S8, S9, S10, S11, T6	Supply	Positive Supply for MGI<0>	1.8V
VDD18_MGI <1>	S13, S14, S15, S16, S17 S18, T18	Supply	Positive Supply for MGI<1>	1.8V
VDD18_MGI <2>	B13, B14, B15, B16, B17, B18, A18	Supply	Positive Supply for MGI<2>	1.8V
VDD18_MGI <3>	B6, B7, B8, B9, B10, B11, A6	Supply	Positive Supply for MGI<3>	1.8V
VDD18_DIG	J20	Supply	Positive Supply for Digital	1.8V
VDD18_AUX	A5	Supply	Positive Supply for Auxiliary	1.8V
VDD18_PLL	O1, O2, O3, O4, P4	Supply	Positive Supply for PLL	1.8V. Use decoupling to GND
VDD18_VCO	M3, N1, N2, N3	Supply	Positive Supply for VCO and Loop Filter	1.8V. Use decoupling to GND
D2P_RFO <2:0>	P7, M7, M7	RFO	MGI00 D2P RF outputs	3 RF outputs to drive 00 Spinwave MAJ
D2P_RFO <5:3>	P14, M14, M17	RFO	MGI01 D2P RF outputs	3 RF outputs to drive 01 Spinwave MAJ
D2P_RFO <8:6>	E14, H14, H17	RFO	MGI02 D2P RF outputs	3 RF outputs to drive 02 Spinwave MAJ
D2P_RFO <11:9>	E11, H11, H10	RFO	MGI03 D2P RF outputs	3 RF outputs to drive 03 Spinwave MAJ
P2D_RFIP/N <0>	P10, Q11	RFI	MGI00 P2D differential RF input	Differential RF input from 00 Spinwave MAJ
P2D_RFIP/N <1>	P17, Q17	RFI	MGI01 P2D differential RF input	Differential RF input from 01 Spinwave MAJ
P2D_RFIP/N <2>	E17, Q17	RFI	MGI02 P2D differential RF input	Differential RF input from 02 Spinwave MAJ
P2D_RFIP/N <3>	E10, Q10	RFI	MGI03 P2D differential RF input	Differential RF input from 03 Spinwave MAJ

Pin Name	Pin No.	Type	Description	Comments
LO	H3	RFIO	Local Oscillator	50Ω termination. This pin acts either as the PLL RF output, either as an RF input reference signal, necessary for MGI00 and MGI01.
D2P_DI18<2:0>	T11, T10, T9	DI	D2P Digital Inputs	MGI00 D2P 3 digital inputs, to set the phase of the corresponding RF outputs. Pulled down internally with 100kΩ.
D2P_DI18<5:3>	T13, T14, T15	DI	D2P Digital Inputs	MGI01 D2P 3 digital inputs, to set the phase of the corresponding RF outputs. Pulled down internally with 100kΩ.
D2P_DI18<8:6>	A13, A14, A15	DI	D2P Digital Inputs	MGI02 D2P 3 digital inputs, to set the phase of the corresponding RF outputs. Pulled down internally with 100kΩ.
D2P_DI18<11:9>	A11, A10, A9	DI	D2P Digital Inputs	MGI03 D2P 3 digital inputs, to set the phase of the corresponding RF outputs. Pulled down internally with 100kΩ.
P2D_DO18\c<0>	T7, T8	DO	P2D Digital Output	MGI00 P2D digital output and its complementary
P2D_DO18\c<1>	T17, T16	DO	P2D Digital Output	MGI01 P2D digital output and its complementary
P2D_DO18\c<2>	A17, A16	DO	P2D Digital Output	MGI02 P2D digital output and its complementary
P2D_DO18\c<3>	A7, A8	DO	P2D Digital Output	MGI03 P2D digital output and its complementary
CS18	E20	DI ¹	Chip Select	Pulled down internally with 200kΩ
SDO18	F20	DO ¹	Serial data output	Maximum load 15pF@50MHz, 5pF@150MHz
SDI18	G20	DI	Serial data input	Pulled down internally with 200kΩ
CLK18	H2	DI	SPI Clock	Pulled down internally with 200kΩ
AD111_READY18	F1	DI	ADC Ready	When 1.8V, ADC output is ready to be read through SPI
RST18	N20	DI	SPI External Reset	1.8V pulse is required (minimum width 1.3ns). When 1.8V → SPI is in reset mode. When 0V → SPI operates normally.
ADR18<3:0>	R20, Q20, P20, O20	DI	Chip Address	Pins are internally pulled-up ²
ATBP	A4	AO	Analog Test Bus Positive	Voltage of measured signal (0V - 1.8V). Measured signal can be one of the following: Analog Test Bus signal, Power Detector positive signal, PLL divided signal, PLL reference signal
ATBN	A3	AO	Analog Test Bus Negative	Voltage of measured signal (0V - 1.8V). Measured signal can be one of the following: Analog Test Bus signal corresponding ground, Power Detector negative signal, AD111_STR signal
XTAL	T3	AI	External XTAL Oscillator Connection	AC coupled internally
CPO	S4	AO	Charge Pump Current Output	Unconnected if not used
VTUNE	L1	AIO	VCO Tunning Voltage Input/Output	Can be used as a test point
VREF	H2	AI	Externally Decoupled VCO Reference Voltage	1u-10uF

¹All digital input and output pins have logic high level of 1.8V.

²To set a Chip Address, the ADR18<3:0> pins are used. All the ADR18 pins are internally pulled up. To set to zero a Chip Address bit, the corresponding ADR18 pin should be connected to PCB ground.

Table 3: Pin description.

8 Typical Performance Characteristics

8.1 D2P

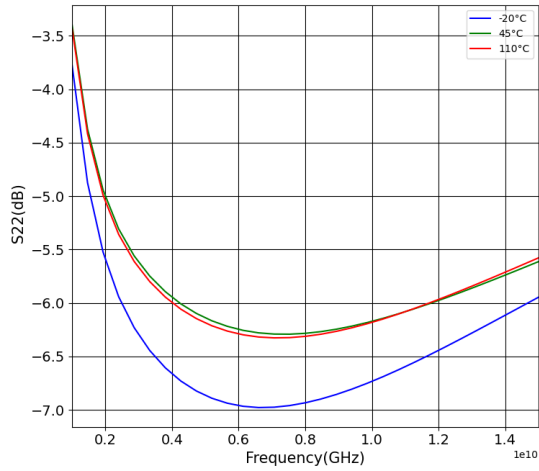


Figure 4: Simulated D2P ANT_DRV_i S_{22} over temperature.

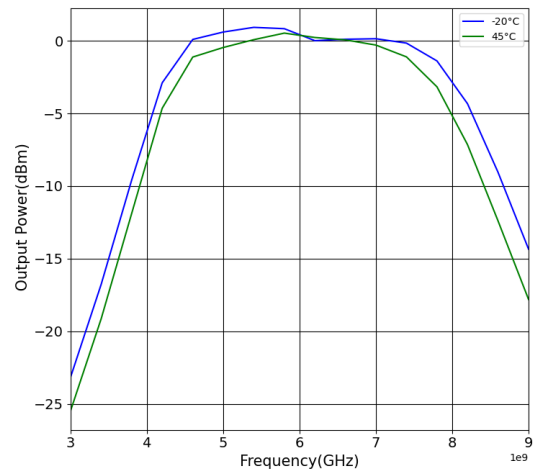


Figure 5: Simulated Output Power over Frequency across temperature.

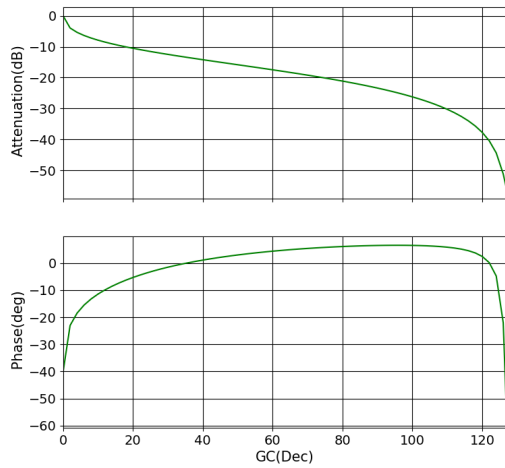


Figure 6: Simulated D2P ANT_DRV_i output attenuation and phase over MGIx_D2P_GCi<6:0>, for D2P_DI18<3*x+i>=0V, at 8GHz.

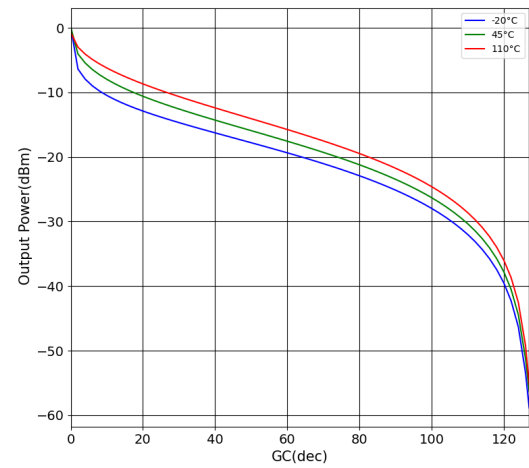


Figure 7: Simulated D2P ANT_DRV_i output power over MGIx_D2P_GCi<6:0> at 6.5GHz.

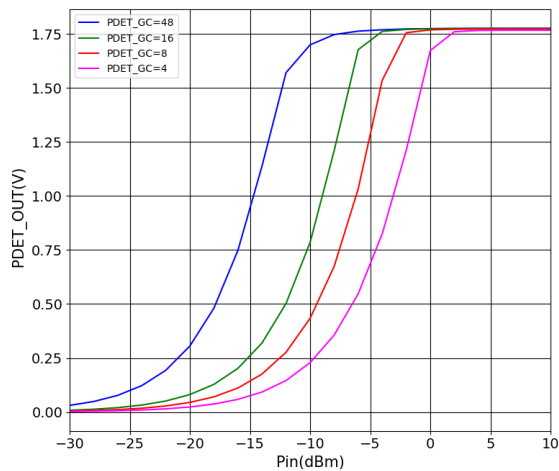


Figure 8: Simulated power detector output voltage over sensed power and PDET_GC<5:0>.

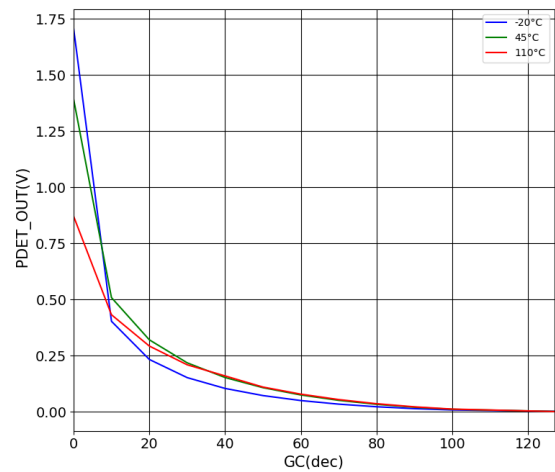


Figure 9: Simulated D2P ANT_DRV_i power detector output over MGIx_D2P_GCi<6:0>, for PDET_GC<5:0>=001000.

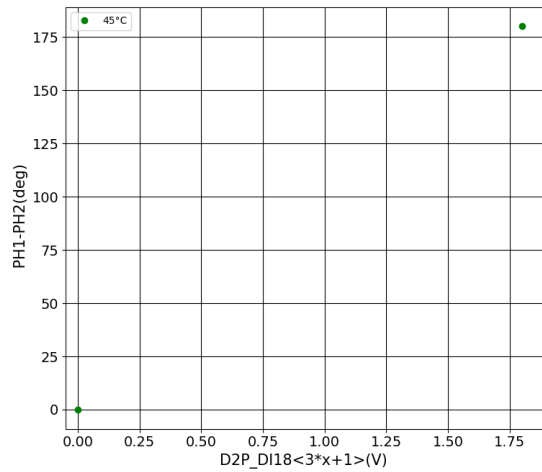


Figure 10: Simulated D2P ANT_DRV1 and ANT_DRV2 phase difference, over D2P_DI18<3*x+1> voltage, when D2P_DI18<3*x+2>=0V (at equal output power).

8.2 P2D

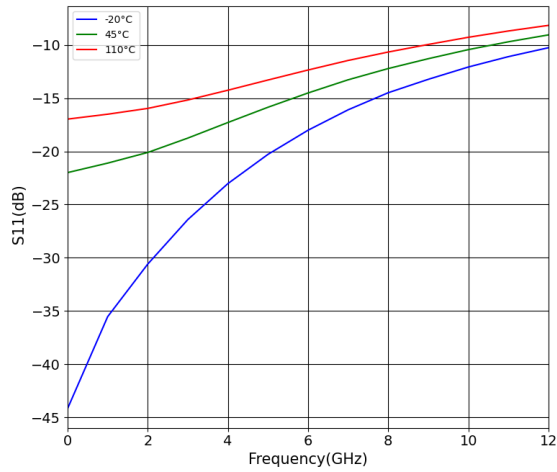


Figure 11: Simulated P2D S_{11} (diff. port) over temperature.

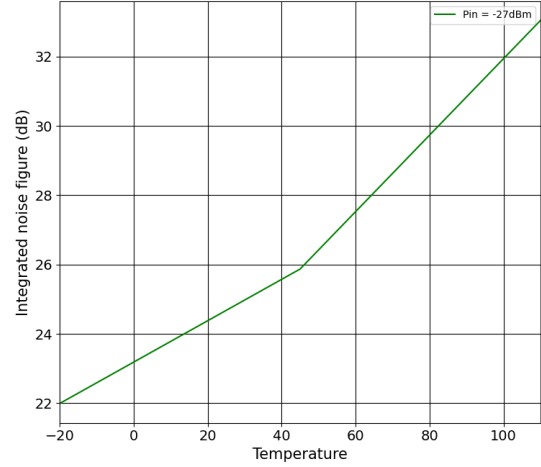


Figure 12: Simulated Integrated Noise Figure for -27dBm P2D input power over temperature, at 8GHz. Sampled differentially at LPF output.

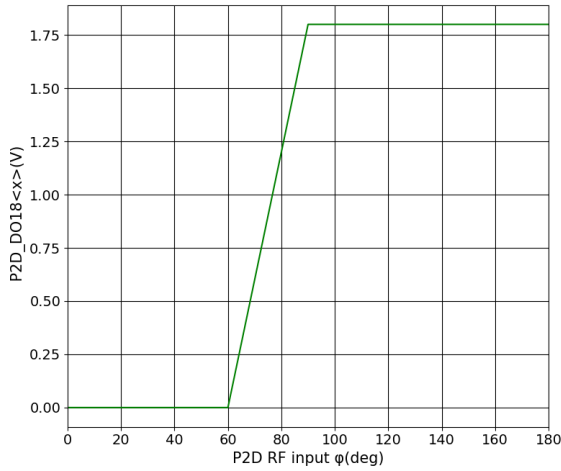


Figure 13: Simulated P2D_DO18<x> pin voltage over P2D RF input phase, for constant PS settings.

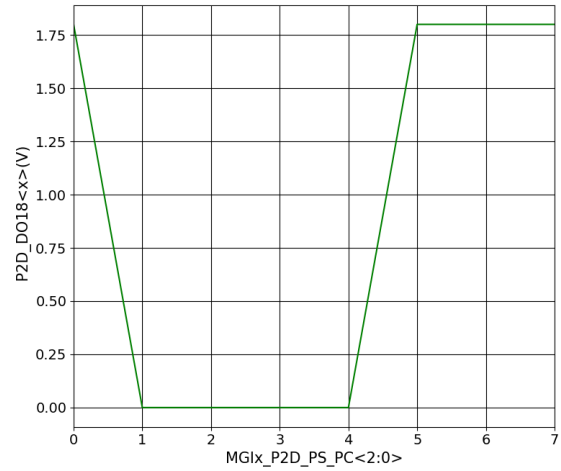


Figure 14: Simulated P2D_DO18<x> pin voltage over MG1x_P2D_PS_PC<2:0>.

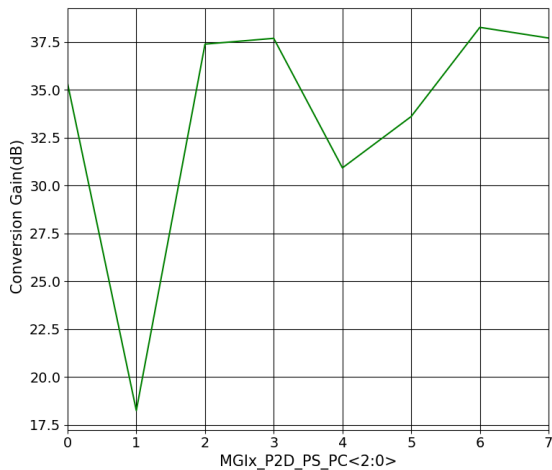


Figure 15: Simulated P2D conversion gain over MG1x_P2D_PS_PC<2:0>.

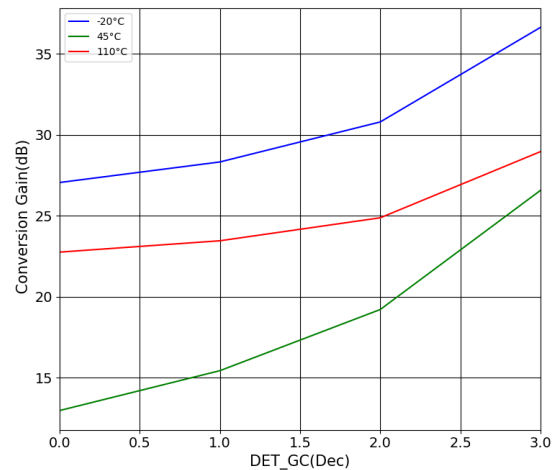


Figure 16: Simulated P2D conversion gain over MG1x_P2D_DET_GCi<1:0> and temperature.

9 Overview

SPIDER APIC 2 consists of:

- 4 Majority Gate Interfaces (MGI_x, where $x = 00/01/02/03$)
 - MGI00, MGI01, MGI02, MGI03 fed either from the PLL, or externally from LO pin.
- Each MGI is comprised of:
 - One D2P block, to excite the SW MAJ inputs,
 - One P2D block, to interpret the SW MAJ output.
- Fractional-N PLL at 5.92 – 6.9GHz
- 4-wire SPI communication with 33 static registers.
- Power detectors in each D2P RF output (12 total).
- 10-bit SAR ADC.
- Analog Test Bus (ATB) in MGI01, PLL, ADC and Bandgap.

SPIDER APIC 2 offers many functionalities:

- ▶ The phase can be inverted in each D2P antenna driver (ANT_DRV) block, by using the D2P_DI18 pins. This makes possible the alternation of the logic information passed in each RF input of a SW MAJ. The gain is invariant in this control.
- ▶ The output power of each D2P ANT_DRV block, and thus each SW MAJ RF input, can be controlled. This control is phase invariant and gives 30dB range.
- ▶ A Phase Shifter that can compensate the unknown phase shift that will occur in the RF signals due to interposer routing and the magnonic chip. Through its phase control settings, it is used to calibrate the MGI.
- ▶ Option to control the active filter gain of the P2D chain, with 12dB range.
- ▶ An integer and fractional-N PLL which offers many functionalities, such as loop bandwidth selection, VCO auto-calibration, external VCO and Loop Filter support and performance optimization through many internal parameters (e.g. bias currents and voltages).
- ▶ An array of up to 16 ICs can be controlled through the same 4-wire SPI. Each IC should have its own Chip Address, which can be given through the ADR18<3:0> pins (hardwired to the PCB).
- ▶ SPI is equipped with the conventional Read and Write operations.
- ▶ Power detection in every D2P Power Amplifier (12 total, 3 per D2P).
- ▶ An ATB that provides easy access to many internal nodes of the MGI01, PLL, ADC and Bandgap, enabling verification, calibration and production testing.
- ▶ An ADC that can measure the ATB and power detector output DC voltages and produce a digital output. These DC voltages can also be measured through the ATBP/N pins if needed.
- ▶ Digital control in bias currents of the MGIs and the ADC, and also in all the LDOs output voltage. These controls provide the option to compensate in corner cases and trade consumption with performance.
- ▶ Option to use CMOS MAJ instead of SW MAJ and MGI analog circuitry.

10 Operation & Digital Controls

10.1 RF Digital Controls

10.1.1 Majority Gate Interface (MGI)

The Majority Gate Interface block is used 4 times inside the *SPIDER APIC 2*. It is the block responsible for communicating with the Spinwave Majority gate (SW MAJ), meaning that *APIC 2* can control maximum 4 SW MAJ gates. An MGI is comprised of the Digital to Phase (D2P) block and the Phase to Digital (P2D) block, as shown in Figure 17. The D2P block is responsible for the excitation of the three inputs of a single SW MAJ, while the P2D block is responsible for interpreting the SW MAJ output. Both these sub-blocks are described thoroughly in the Sections 10.1.2 and 10.1.3, respectively.

In order for an MGI to operate properly, an RF input signal is needed in order to act as a reference. This is provided through the PLL. This reference signal is split into 4 signals inside the D2P, three to be used to excite a specific SW MAJ, and one to be used from the P2D in order to interpret a SW MAJ output. The three excitation signals follow separate but completely identical paths before reaching the dedicated D2P_RFO pin, meaning that their phase at the output will be identical, unless it is intentionally inverted by the user through the D2P_DI18 pins. As for the interpretation of a SW MAJ output, this RF output must be given as a differ-

ential input to the P2D block through the P2D_RFIP/N pins. Then it is mixed with the Phase Shifter differential RF output, which is produced by the 4th reference signal propagated by the D2P. After mixing these RF signals, the product is being filtered and compared, and as a result the desired information is translated in the logic domain. This logic interpretation of the SW MAJ and its complementary, are then available to the P2D_DO18 and P2D_DO18c pins. Note that calibration is needed in order for the P2D interpretation to be reliable, as described in Section 10.2.2.

Each MGIX (where $x=00/01/02/03$) has 5 digital pins. The three input pins D2P_DI18<[3*x+2]:[3*x]> that are used as controls for the phase inversion decision of the corresponding RF SW MAJ input, and the two output pins P2D_DO18<x> and P2D_DO18c<x> for the P2D interpretation of the SW MAJ output and its complementary, respectively. It also has 5 RF pins, D2P_RFO<[3*x+2]:[3*x]> for the 3 outputs to the SW MAJ (D2P outputs), and P2D_RFIP/N<x> for the differential input from SW MAJ (P2D input). There are many digital controls for circuitry included in the MGI and are all described in the D2P, P2D and PS sections.

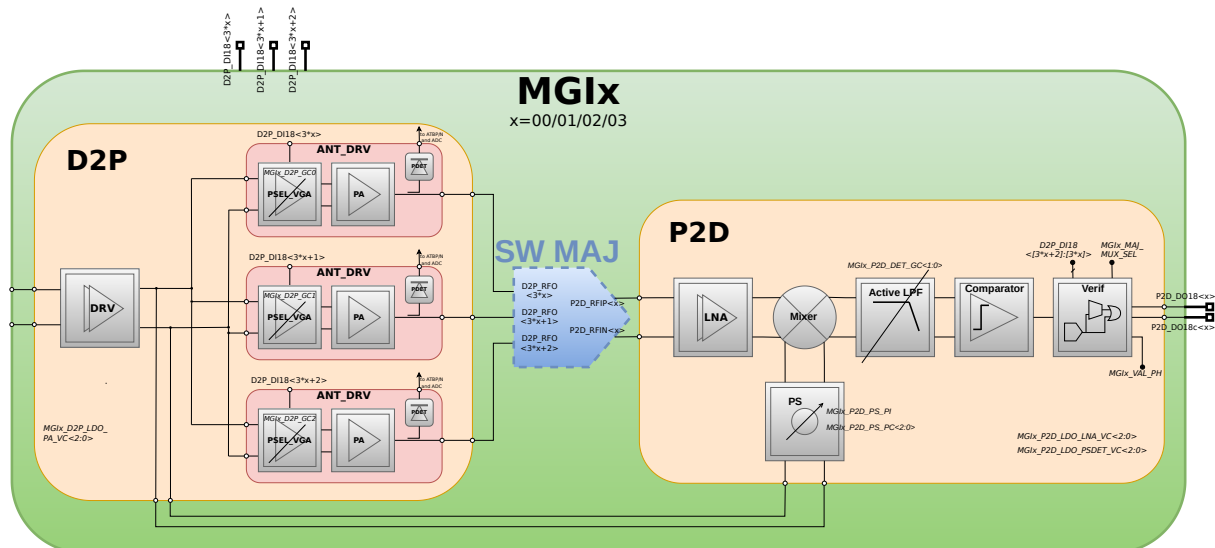


Figure 17: MGI block diagram.

10.1.2 Digital to Phase (D2P)

The Digital to Phase block is responsible for the excitation of the three inputs of a SW MAJ. It is comprised of one driver (DRV) and three antenna driver (ANT_DRV) blocks, with separate phase and gain control utilities for the latter. ANT_DRV is comprised of two stages, the phase select and variable gain amplifier (PSEL_VGA) block and the power amplifier (PA) block. In each PA output a power detector is connected. The D2P block diagram is depicted in Figure 18.

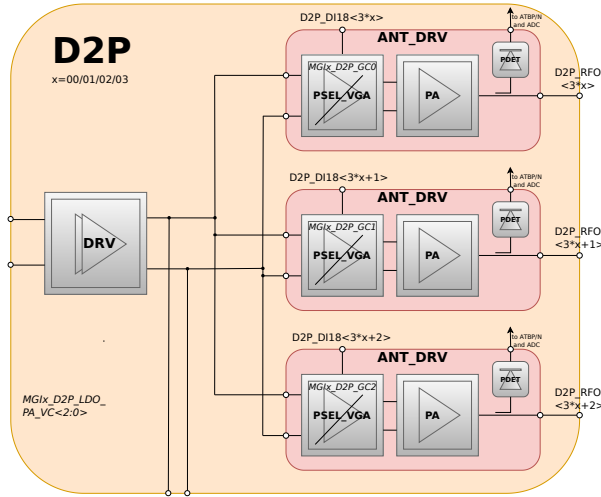


Figure 18: D2P block diagram.

A differential RF reference signal is given as input to the D2P, through the PLL. The D2P is configured to provide a high input impedance for maximum voltage transfer from the PLL driver. The input signal is then amplified through the DRV block in order to propagate it to three ANT_DRV blocks and also to the Phase Shifter (section 10.1.4). The signals passing through the ANT_DRV blocks follow identical paths, meaning that their phase at the output will be identical, unless it is intentionally inverted through the D2P_RFO pin by the user. In the PSEL_VGA block both gain control and phase inversion of the signal can be performed. Then the signal reaches the final PA stage, which provides a differential to single ended conversion without the use of a balun, and drives a single-ended antenna through the corresponding D2P_RFO pin (12 total, 3 per D2P). The PA block has fixed power gain, letting the input swing of the signal to control the power at the load. The maximum power that it can deliver to a 50Ω load is 0dBm. Finally, the power delivered can be detected internally through power detectors which are connected to each PA output (Section 10.3.3).

Phase and Gain Control

Phase and gain control are applied to the ANT DRV, and more specifically in the PSEL_VGA block. This block

is repeated three times inside a D2P block, and it offers a phase inversion control (180° phase shift) for the corresponding RF signal, as well as extensive control in the gain and hence the output power delivered to the corresponding antenna.

The phase inversion of all the RF signals can be controlled either externally through the corresponding D2P_DI18<i> pins (Table 4) or internally through the SPI via the MGIx_D2P_PH_SEL<2:0> bits (Table 5). The choice between either one is configured via PHASE_CTRL_SEL bit, set to 0 for internal control or to 1 for external (6). It must be noted that since there are 4 different MGIs in the APIC 2, there are 12 D2P_DI18 pins total. D2P_DI18<2:0> pins control the MGI00, D2P_DI18<5:3> pins control the MGI01, D2P_DI18<8:6> pins control the MGI02 and D2P_DI18<11:9> pins control the MGI03.

Phase control pin	Voltage applied to pin ¹	Phase shift on D2P RF output
D2P_DI18<i> ²	0V	0°
	1.8V	180°

¹Default value is 0V, pulled down internally.

²i=0/1/.../11.

Table 4: D2P RF phase inversion through D2P_DI18<i> pins.

MGIx_D2P_PH_SEL<i> ¹	Phase shift on MGIx D2P, ANT_DRVi RF output
0	0°
1 ²	180°

¹x=00/01/02/03 and i=0/1/2.

²Default value.

Table 5: D2P RF phase inversion through MGIx_D2P_PH_SEL<2:0> bits.

PHASE_CTRL_SEL	D2P RF output phase control selection
0 ¹	Internal (SPI)
1	External (APIC2 pins)

¹Default value.

Table 6: D2P RF output phase control selection.

The variable gain is controlled internally through the bits MGIx_D2P_GC<6:0> (Table 7). Normally, gain control requires calibration using look-up tables, to achieve a linear behavior with a constant attenuation step. The GC is finely adjustable (7 control bits) in order to allow high resolution after calibration. Please refer to

Section 10.2.1 for more information about gain calibration.

Voltage applied at D2P_DI18<3*x+i>	GC bits ¹	Bit Value Range (DEC)	Attenuation Range (dB)
0V	MGIx_D2P_GCi<6:0> ²	0-127	0 - 30dB
1.8V	MGIx_D2P_GCi<6:0>	0-127	0 - 30dB

¹Default value is <0000000>.

²x=00/01/02/03 and i=0/1/2.

Table 7: D2P Gain Control.

Gain control selection is not independent of the phase inversion control. It is apparent in Table 7 that when D2P_DI18<3*x+i> pin is 0V or 1.8V, then low decimal values of the MGIx_D2P_GCi<6:0> bits correspond to low attenuation of the ANT_DRV_i output power, and high values correspond to high attenuation. Figure 7

One more thing that should be noticed about the gain control of an ANT_DRV, is that it is not phase invariant. This means that when the gain control settings of an ANT_DRV change, then the phase of the corresponding output RF signal also changes by a few degrees. The phase change is significant, and may affect the MGI calibration procedure results (Section 10.2.2). The amount of phase shift is 45° over a 30dB gain control range, as can be seen in Figures 6. This phase shift doesn't affect the phase inversion control.

Bias Controls

D2P has two LDOs, one for supplying the PA0 and one for supplying the PAs 1 and 2. All the LDO voltages can be controlled digitally through SPI, by the MGIx_D2P_LDO_PA_VC<2:0> bits. These controllable voltages provide the option to optimize performance, compensate in corner cases alongside with some extra flexibility for fine adjustments. The following tables describe in detail the voltage control settings.

All the D2P and P2D bias currents are controllable, but not independently from one another. They can be controlled through the bits MGI_BIAS_CC<2:0>, described in Section 10.3.1.

MGIx ¹ _D2P_LDO_PA_VC <2:0>	MGIx D2P PAs V _{supply}
000	1.17V
001	1.12V
010	1.08V
011	1.04V
100 ²	1V
101	0.96V
110	0.92V
111	0.89V

¹x=00/01/02/03.

²Default value.

Table 8: Power Amplifiers LDO supply voltage control.

Power Down Controls

All the components of the D2P block can be powered down separately, by configuring the appropriate bits. In order for one D2P to operate properly, these bits must be set to 0.

Bit Name ²	Description
MGIx ¹ _PD_D2P_BIAS	Power Down D2P BIAS
MGIx_PD_D2P_LDO_DRV	Power Down D2P driver LDO
MGIx_PD_D2P_LDO_PA	Power Down D2P PA LDO
MGIx_PD_D2P_DRV	Power Down D2P DRV
MGIx_PD_D2P_PSEL_VGA<0>	Power Down D2P PSEL_VGA 0
MGIx_PD_D2P_PSEL_VGA<1>	Power Down D2P PSEL_VGA 1
MGIx_PD_D2P_PSEL_VGA<2>	Power Down D2P PSEL_VGA 2
MGIx_PD_D2P_PDET<0>	Power Down D2P PDET 0
MGIx_PD_D2P_PDET<1>	Power Down D2P PDET 1
MGIx_PD_D2P_PDET<2>	Power Down D2P PDET 2
MGIx_PD_D2P_PA<0>	Power Down D2P PA 0
MGIx_PD_D2P_PA<1>	Power Down D2P PA 1
MGIx_PD_D2P_PA<2>	Power Down D2P PA 2

¹x=00/01/02/03.

²All signals are active high. Their default values are 1.

Table 9: D2P power down control bits.

10.1.3 Phase to Digital (P2D)

The Phase to Digital block is responsible for interpreting the SW MAJ output. Its architecture is based on a direct conversion receiver (Figure 19), which down-converts an RF signal to a baseband signal that contains the phase information of the RF input. The main blocks of the P2D chain are an LNA, an active mixer, an active low pass filter (LPF) and a comparator. There is also the Phase Shifter that can be considered as an autonomous block (Section 10.1.4) and the Verif block, which contains digital logic that provides extra functionalities.

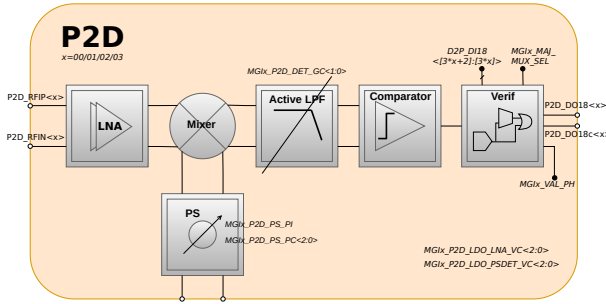


Figure 19: P2D block diagram.

A SW MAJ produces a differential RF signal, which is given as an input to the corresponding P2D through the pins P2D_RFIP/N<x> (where x=0/1/2/3). Then this signal is amplified through the LNA block, which is designed considering 35Ω input impedance per single ended input. The LNA differential output is passed to the first input of the mixer. The other differential input of the mixer is the output of the PS block. By mixing these RF signals, two RF signals are produced that have the wanted information on their DC voltage level. So, the differential output of the mixer is passed to an active LPF, and then the two outputs of the LPF are compared with a comparator. The logic output of the comparator is the interpretation of the SW MAJ output. This interpretation has no special meaning until calibrating the MGIX through the corresponding Phase Shifter, as described in Section 10.2.2. This logic output is available at the corresponding P2D_DO18<x> and complementary P2D_DO18c<x> pins as well as through the SPI via the MGI_P2D_DO and MGI_P2D_DOc bits.

As it can be seen in the P2D block diagram (Figure 19), a block called Verif exists after the comparator. This block contains simple digital logic circuitry that may be found useful for MGIX operation verification. Firstly, it contains a 3 input MAJ gate implemented in CMOS logic, which takes the same digital inputs as the D2P block (i.e. the ones given from the D2P_DI18<[3*x+2]:[3*x]> pins), and its output can be connected to the P2D_DO18<x> and P2D_DO18c<x> pins by properly setting the bit MGIX_MAJ_MUX_SEL (Table 10). This means that

there is the option to bypass, if needed, the whole P2D and D2P analog circuitry, replacing the SW MAJ gate with the CMOS one.

MGIX ¹ _MAJ_MUX_SEL	Operation
0 ²	P2D output to P2D_DO18<x> pin ³
1	CMOS MAJ output to P2D_DO18<x> pin

¹x=00/01/02/03.

²Default value.

³After calibration, P2D output = SW MAJ output.

Table 10: Majority gate selection.

Verif block also contains a 2-input XNOR gate that, when MGIX¹_MAJ_MUX_SEL=0, it compares the CMOS MAJ output with the P2D output. The P2D output will be equal to SW MAJ output after proper MGIX calibration. This way, the SW MAJ can be compared with the CMOS MAJ. When the MAJ gates outputs are equal, the bit MGIX_VAL_PH, that is the MGIX XNOR gate output, goes to logic 1, and when not it goes to logic 0. The bit MGIX_VAL_PH is an SPI output, and can only be read through the SPI. When MGIX¹_MAJ_MUX_SEL=1, the MGIX_VAL_PH bit is not valid (it should always be equal to 1).

Condition ¹	MGIX ² _VAL_PH
P2D output doesn't match with CMOS MAJ output	0
P2D output and CMOS MAJ output are the same	1

¹When MGIX_MAJ_MUX_SEL=0, else not valid.

²x=00/01/02/03.

Table 11: VAL_PH output bit.

Gain Control

There is the option to control the active LPF gain of the P2D chain, through the bits MGIX_P2D_DET_GC<1:0> (Table 12). This control may be found extra useful in case of excessive LO self-mixing.

MGIX ¹ _P2D_DET_GC<1:0>	Conversion Gain
00	MAX - 12dB
01	MAX - 10dB
10 ²	MAX - 7dB
11	MAX

¹x=00/01/02/03.

²Default value.

Table 12: P2D conversion gain control.

Bias Controls

P2D has two LDOs, one for supplying the LNA block and one for supplying the Phase Shifter and its Mixer driver. All the LDO voltages can be controlled digitally through SPI. The LNA LDO by the **MGIx_P2D_LDO_LNA_VC<2:0>** bits and the other by the **MGIx_P2D_LDO_PSDET_VC<2:0>**. These controllable voltages provide the option to optimize performance and compensate in corner cases. The following tables describe in detail the voltage control settings.

All the D2P and P2D bias currents are controllable, but not independently from one another. They can be controlled through the bits **MGI_BIAS_CC<2:0>**, described in Section 10.3.1.

MGIx¹_P2D_LDO_LNA_VC <2:0>	MGIx P2D LNA V_{supply}
000	1.17V
001	1.12V
010	1.08V
011	1.04V
100 ²	1V
101	0.96V
110	0.92V
111	0.89V

¹x=00/01/02/03.

²Default value.

Table 13: Low Noise Amplifier LDO supply voltage control.

MGIx¹_P2D_LDO_PSDET_VC<2:0>	MGIx P2D PSDET V_{supply}
000	1.17V
001	1.12V
010	1.08V
011	1.04V
100 ²	1V
101	0.96V
110	0.92V
111	0.89V

¹x=00/01/02/03.

²Default value.

Table 14: Phase shifter and its Mixer driver LDO supply voltage control.

Power Down Controls

All the components of the P2D block can be powered down, by configuring the appropriate bits. In order for the P2D to operate properly, these bits must be set to 0.

Bit Name²	Description
MGIx¹_PD_P2D_BIAS	Power Down P2D BIAS
MGIx_PD_P2D_LDO_LNA	Power Down P2D LNA LDO
MGIx_PD_P2D_LDO_PSDET	Power Down P2D PS and Mixer driver LDO
MGIx_PD_P2D_DET	Power Down P2D Detector (Mixer, Active LPF and comparator)

¹x=00/01/02/03

²All signals are active high. Their default values are 1.

Table 15: P2D power down control bits.

10.1.4 Phase Shifter (PS)

The Phase Shifter (PS) is situated inside the P2D block, but it can be considered as an autonomous block. It takes a differential RF input from the D2P driver block, and then it produces a phase shifted differential RF output, by properly phase shifting the input signal. The amount of phase shift can be controlled through the SPI, as described in the following paragraphs. The produced RF signal is forwarded to a driver and then enters the active mixer of the P2D, in order to be mixed with the P2D differential RF input (Figure 19).

The PS is configured as a delay line, in which the reference RF signal is delayed with a steady delay. The structure implemented provides an initial amplifying stage in order to create a sharp square wave, followed by coarse and fine phase shift sections. The coarse phase shift section provides phase inversion (i.e. 180°). The fine shift section provides 45° of phase shift under typical temperature (45°C) and process conditions. The coarse section was implemented to assure that a complete 360° of phase shift can be covered under process voltage and temperature (PVT) variations.

Phase Controls

As already mentioned, PS provides a phase inversion control and a fine shift control. The first one is controlled by the bit **MGIX_P2D_PS_PI** and the second one by the bits **MGIX_P2D_PS_PC<2:0>** (Tables 16 and 17 respectively). The behavior of the PS for all the possible combinations of the aforementioned settings and under typical PVT conditions are shown in Table 18.

MGIX ¹ _P2D_PS_PI	Phase Shift (°)
0 ²	0°
1	180°

¹x=00/01/02/03.

²Default value.

Table 16: Phase inversion PS setting.

MGIX ¹ _P2D_PS_PC<2:0>	Phase Shift (°)
000 ²	0°
001	45°
010	135°
011	180°
100	225°
101	270°
110	315°
111	360°

¹x=00/01/02/03.

²Default value.

Table 17: Fine shift PS setting, under typical PVT conditions.

MGIX ¹ _P2D_PS_PI	MGIX_P2D_PS_PC<2:0>	Phase Shift (°)
0 ²	000	0°
0	001	45°
0	010	90°
0	011	135°
0	100	180°
0	101	225°
0	110	270°
0	111	315°
1	000	180°
1	001	225°
1	010	270°
1	011	315°
1	100	0°
1	101	45°
1	110	90°
1	111	135°

¹x=00/01/02/03.

²Default values.

Table 18: Phase shift for all PS setting combinations, and under typical PVT conditions.

It must be noted that the 45° phase step of the setting **MGIX_P2D_PS_PC<2:0>**, is susceptible in process and temperature variations. In Table 17 an entire 360° cycle is covered, but it is possible in extreme PVT conditions for the step to be even 35°, meaning that it will not be able to cover an entire cycle. In this case, the phase inversion setting helps to cover an entire 360° cycle. Still, without knowing the exact PVT conditions, the exact phase step given by the fine PS setting will not be known.

Bias and Power Down Controls

The supply voltage of the PS is produced from an LDO, which also supplies its Mixer driver. This is one of the two LDOs inside the P2D block. PS can only be powered down through this LDO, which is powered down by setting the **MGIX_PD_P2D_LDO_PSDT** bit equal to 1 (Table 15). The supply voltage of the PS can also be adjusted through the LDO, by the bits **MGIX_P2D_LDO_PSDT_VC<2:0>** (Table 14).

10.2 Calibration

There are two different types of calibration required by the SPIDER APIC 2. The first one is the D2P antenna driver (ANT_DRV) gain calibration, which refers to the selection of the optimal values of gain settings in order to achieve linear control and constant resolution. The second one is the phase shifter calibration of an MGI. This calibration is achieved by compensating through the PS for all the phase shift that occurs due to interposer routing and the SW MAJ chip, and is mandatory in order for the P2D to decode properly the SW MAJ output.

10.2.1 D2P Gain Calibration

Gain calibration applies to all D2P antenna drivers (12 total), by using the **MGIx_D2P_GCi<6:0>** bits (where $x=00/01/02/03$ and $i=0/1/2$) described in Section 10.1.2. By following the procedure described below, the user can calibrate the gain of one D2P ANT_DRV, but the resulting look-up tables (LUTs) can be used for all twelve D2P ANT_DRVs.

The **MGIx_D2P_GCi<6:0>** bits affect the D2P ANT_DRV i output power when the D2P_DI18<3*x+i> pin is set to 0V or 1.8V (Figure 20). Table 19 provides the recommended values (derived from simulations) for all the D2P GCs, for D2P_DI18 at 0V and 1.8V respectively, and for gain calibration step equal to 1dB.

Calibration procedure:

A typical way to calibrate gain is the following. Sweep the k-bit digital value of GCx from min to max $\{0, 1, \dots, 2^k-1\}$ and measure the attenuation at each step. Then, given the desired attenuation range and resolution (e.g. 0.5dB/step), store in a LUT only those settings that correspond to the attenuation points that best fit to the ideal curve. One way to evaluate the resulting curve with respect to the ideal, is to use some statistical/numerical measure such as the rmsError, defined as:

$$rmsError_{GC} = \sqrt{\frac{1}{N} \sum_{i=0}^{N-1} (Atten_{ideal}(i) - Atten_{real}(i))^2}$$

where N is the total number of steps/points after calibration.

It must be noted that the attenuation step value is selected by the user. The recommended attenuation step is equal or larger than 0.5dB, because for smaller step sizes the rmsError becomes comparable to the mean step size.

Example:

Calibrating GC in MGI01 D2P ANT_DRV2 block, controlled by bits **MGI01_D2P_GC2<6:0>**, with 0 or 1.8V at D2P_DI<5> pin, for 30dB attenuation range and 1dB resolution.

Step1:

Sweep **MGI01_D2P_GC2<6:0>** in the range $\{0,1,\dots,127\}$ and then plot the attenuation over **MGI01_D2P_GC2<6:0>** curve, as in Figure 20.

Step2:

Store optimal **MGI01_D2P_GC2** values in a LUT, as in Table 19. Optimal GC values are the ones that minimize the difference between the actual attenuation and the ideal attenuation.

This method gives a total attenuation range of 30dB, meanStep value of -1dB and an rmsError of 0.2dB.

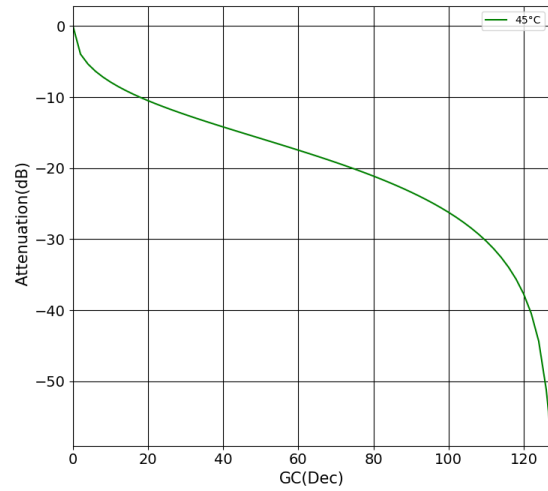


Figure 20: Uncalibrated attenuation over MGIx_D2P_GCi bits, at 6.5GHz, and with D2P_DI18<3*x+i> pin at 0V or 1.8V.

Target Attenuation (dB)	Simulated Attenuation ¹ per GC (dB) when D2P_DI18<3x+i>=0V	MGIx_D2P_GCi ² (HEX)
0	0	00
1	0.993	01
2	1.987	02
3	2.844	04
4	3.774	07
5	4.992	0C
6	5.994	11
7	6.893	16
8	7.888	1C
9	8.985	23
10	9.902	29
11	10.967	30
12	11.895	36
13	12.850	3D
14	13.849	42
15	14.908	48
16	15.855	4D
17	16.872	52
18	17.987	57
19	18.966	5B
20	20.045	5F
21	20.933	62
22	21.919	65
23	23	68
24	23.811	6A
25	24.694	6C
26	25.671	6E
27	26.776	70
28	27.39	71
29	28.74	73
30	30.335	75

¹ rmsError is 0.19dB.

² Default value is 00, and corresponds to 0dB attenuation.

Table 19: MGIx_D2P_GCi<6:0> values for a 1dB step gain calibration, when corresponding D2P_DI18<3x+i> pin is at 0V.

10.2.2 MGI Calibration

The information in a SW MAJ is hidden in the phase of its RF signal inputs and output. The MGI D2P block has the capability of exciting all the 3 inputs of the SW MAJ with RF signals that have the same (e.g. logic 0), or opposite (e.g. logic 1) phase. Then the SW MAJ produces according to its inputs an RF output, that has the information inside its phase. The P2D block is capable of detecting this signal, but is not capable of guessing by itself if the phase of the SW MAJ RF output corresponds to a logic 0 or a logic 1. So, a calibration cycle is needed to be done in an MGI, and more specifically in the corresponding Phase Shifter block, in order for the P2D to recognize properly some phases as a logic 0 (e.g. from ϕ to $\phi + 180^\circ$), and the remaining ones as a logic 1 (e.g. from $\phi + 180^\circ$ to $\phi + 360^\circ$).

Ultimate goal of this calibration is to conclude in some specific Phase Shifter settings. When these settings are applied, the corresponding P2D block will interpret properly the SW MAJ gate output in the logic domain. The SW MAJ gate output is dependent from its inputs (given by the D2P block), according to the truth table 20.

Inputs			Output
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 20: Majority gate truth table.

The calibration procedure described below is valid for one MGI only. If another MGI has the exact same phase delays introduced from the external interconnections (interposer) and the SW MAJ, then the same Phase Shifter settings can be applied to this MGI too. If this is the case for all the 4 MGIs of the SPIDER APIC 2, then the same Phase Shifter settings will apply to all the 4 MGIs, and thus the calibration procedure will need to be done only once.

Also, this calibration procedure is absolutely valid only for a specific D2P gain control attenuation. That is because the D2P gain control (bits MGIx_D2P_GCi<6:0>) is not phase invariant. It introduces a 15° phase shift over a 30dB gain control range, as shown in Figures 6. Though, it is recommended to firstly execute gain calibration (as described in Section 10.2.1) and then execute the MGI calibration for a desired specific attenuation. It should be noticed, that changing attenuation doesn't necessarily means that the

MGI calibration will become invalid, since the phase shift that is introduced isn't that significant, especially in close attenuation values.

Calibration procedure:

Step1:

Power-on the APIC 2 and the MGIx ($x=00/01/02/03$) that needs calibration (Section 10.1). It is assumed that the D2P is enabled and drives with success the SW MAJ, and also that P2D is enabled and able to read the SW MAJ output which is not calibrated yet.

Step2:

Set a known input to the SW MAJ, through the pins D2P_DI18<i> (where $i=[3*x]/[3*x+1]/[3*x+2]$). MGIx_D2P_GCi<6:0> bits should target a specific attenuation, and should also change according the corresponding D2P_DI18<i> pin value.

Step3:

Sweep MGIx_P2D_PS_PI and MGIx_P2D_PS_PC<2:0> bits as shown in Table 21 and measure the corresponding P2D_DO18<x> pin at each step. Store the results in a similar table. Increasing the value of MGIx_P2D_PS_PC setting corresponds to phase shift increment, while the bit MGIx_P2D_PS_PI is used to invert the phase.

Step4:

From the resulting table, select the PS settings that satisfy the following:

1. Result to the correct majority gate output, according to the input that was inserted in Step2 (Table 20)
2. Are the most middle ones in a group of consecutive correct results
3. Have not failed Step5

Step5:

Keep the PS settings selected in Step4, sweep all the possible combinations of D2P_DI18<i> pins, and verify that the SW MAJ produces the expected outputs, as in Table 20. If so, the calibration has finished.

Step6:

If Step5 fails, return to Step4. Repeat until the proper PS settings are found.

D2P_DI18<[3x+2]:[3x]>	MGIX_P2D_PS_PI ¹	MGIX_P2D_PS_PC <2:0>	P2D_DO18<x>	Step4 selection order
011	0	000	0	
	0	001	0	-
	0	010	1	4
	0	011	1	1
	0	100	1	5
	0	101	0	-
	0	110	0	-
	0	111	0	-
	1	000	1	3
	1	001	1	6
	1	010	0	-
	1	011	0	-
	1	100	0	-
	1	101	1	7
	1	110	1	2
	1	111	1	8

¹x=00/01/02/03.

Table 21: PS setting calibration LUT example, for 011 SW MAJ input.

10.3 Auxiliary Digital Controls

SPIDER APIC 2 accommodates several auxiliary blocks, including a bandgap reference, a Successive Approximation Register Analog-to-Digital Converter (SAR ADC), power detectors and baseband circuits. It also includes an Analog Test Bus (ATB), which allows access to selected internal nodes of the MGI01. The auxiliary blocks are described in detail in the following subsections.

10.3.1 Biasing and readout

The bandgap is the main biasing source of the IC, providing constant DC currents over temperature and supply variations. Therefore it must be activated at all times during operation, by setting the **PD_BG** bit to 0 (Table 24).

The bias current of the MGIs and the ADC is variable and can be adjusted digitally through SPI. Adjustable current provides the option to compensate in corner cases and trade consumption with performance. Table 22 describes in detail the current control settings of the MGIs through the **MGI_BIAS_CC<2:0>** bits. Table 23 describes the current control settings of the ADC, through the **AD111_BIAS_CC<2:0>** bits. There is also the option to power down these bias currents by using the bits **PD_MGI_BIAS** and **PD_AD111_BIAS** respectively (Table 24).

MGI_BIAS_CC<2:0>	MGI BIAS I_{DC}
000	$I_{NOM} - 20\%$
001	$I_{NOM} - 10\%$
010	$I_{NOM} = 50\mu A$
011	$I_{NOM} + 10\%$
100	$I_{NOM} + 20\%$
101	$I_{NOM} + 30\%$
110	$I_{NOM} + 30\%$
111	$I_{NOM} + 30\%$

Table 22: Bias current control for all the MGIs.

AD111_BIAS_CC<2:0>	AD111 BIAS I_{DC}
000	$I_{NOM} - 20\%$
001	$I_{NOM} - 10\%$
010	$I_{NOM} = 50\mu A$
011	$I_{NOM} + 10\%$
100	$I_{NOM} + 20\%$
101	$I_{NOM} + 30\%$
110	$I_{NOM} + 30\%$
111	$I_{NOM} + 30\%$

Table 23: ADC bias current control.

PD bits¹	Description
PD_BG	If 1, bandgap is powered down
PD_MGI_BIAS	If 1, all the MGIs bias currents are powered down
PD_AD111_BIAS	If 1, AD111 bias current is powered down

¹Default values of PD bits are 1.

Table 24: Auxiliary biasing power down bits.

In order to properly read out through the ATBP/N pins or the ADC, care must be given in the interconnections shown in Figure 21. Through the ATBP/N pins there is the capability of reading the ATB output, the power detector (PDET) output and some other signals (PLL Fdiv, PLL Fref and ADC Start). These pins can also be used as an ADC external input if needed.

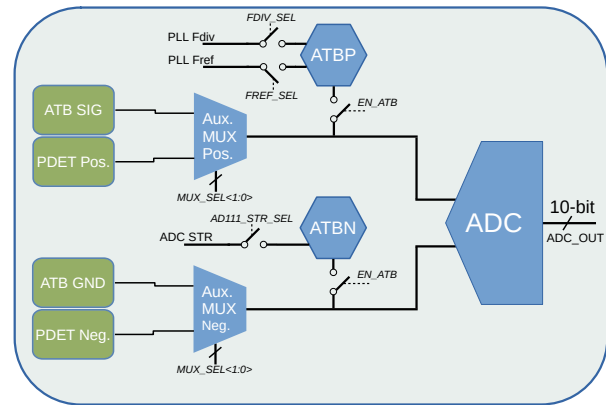


Figure 21: Auxiliary Output Block Diagram

The usage of the control bits **EN_ATB**, **FDIV_SEL**, **FREF_SEL**, **AD111_STR_SEL** is shown in Figure 21, and is explained through the following tables. Note that when one of these control bits is set to 1, the others must be set to 0.

EN_ATB	Operation
0 ¹	Disconnect ATBP/N pins from AUX multiplexer and ADC
1	Connect ATBP/N pins to AUX multiplexer and ADC

¹Default value.

Table 25: EN_ATB bit settings.

FDIV_SEL	Operation
0 ¹	Corresponding buffer goes to High Z output
1	Pass the PLL divided frequency to ATBP pin

¹Default value.

Table 26: FDIV_SEL bit settings.

FREF_SEL	Operation
0 ¹	Corresponding buffer goes to High Z output
1	Pass the XTAL reference frequency of the PLL to ATBP pin

¹Default value.

Table 27: FREF_SEL bit settings.

AD111_STR_SEL	Operation
0 ¹	Corresponding buffer goes to High Z output
1	Pass the ADC "start" signal to ATBN pin

¹Default value.

Table 28: AD111_STR_SEL bit settings.

By setting properly the **MUX_SEL<1:0>** bits, either the ATB output or the power detector output can be selected to be read from the ATBP/N pins or the ADC. Note that setting 11 will lead to shortcircuits, and thus its invalid. All the possible settings of **MUX_SEL<1:0>** can be found in Table 29.

MUX_SEL<1:0>	AUX MUX Selection
00 ¹	No selection
01	ATB
10	PDET
11	Invalid

¹Default value.

Table 29: Auxiliary multiplexer selection.

As for the AD111_READY18 pin, it can be used to measure the corresponding signal, but the **EN_AD111_READY18** bit should be set to 1, as shown in the following table.

EN_AD111_READY18	Operation
0 ¹	Corresponding buffer goes to High Z output
1	Pass the ADC "ready" signal to pin AD111_READY18

¹Default value.

Table 30: EN_AD111_READY18 bit setting.

10.3.2 Analog Test Bus (ATB)

The ATB allows the user to have access and to measure selected internal nodes of the IC. More specifically, these nodes lay inside the MGI01, the PLL, the bandgap and the ADC. The selection of the desired internal node is controlled by the bits **ATB_EN<27:18>** for the PLL, **ATB_EN<16:4>** for the MGI01, and **ATB_EN<3:1>** for three AUX signals, as shown in Table 32. Only

one internal node should be selected at a time, otherwise shortcircuits will occur. All the bits of the vector **ATB_EN<28:0>** refer to internal nodes, except the **ATB_EN<17>** and **ATB_EN<28>** which refer to switches that give access to a team of nodes. These switches should be selected only when an internal node of their team is selected to be measured. In order to measure a node inside MGI01, only this node should be selected by setting the corresponding bit equal to 1, and also the **ATB_EN<17>** bit should be set to 1. In order to measure a node inside PLL, only this node should be selected by setting the corresponding bit equal to 1, and also the **ATB_EN<28>** bit should be set to 1. Note that only one switch should be selected at a time.

As shown in Figure 21, there are two possible ways to measure the voltage value of a node; either by measuring at the ATBP and ATBN pins, or by using the integrated ADC. The bits **MUX_SEL<1:0>** should be set to 01 in either case. If the ATBP/N pins are used, the **EN_ATB** must be set to 1, and then the ATBP pin will output the signal of the measured node and the ATBN pin will output the corresponding ground of the signal. If the ADC is used, the **EN_ATB** must be set to 0, and then proper reading of the ADC output through SPI is needed.

10.3.3 Power Detector (PDET)

Each MGI is equipped with three RF power detectors, one at each D2P PA output, in order to sense the power which is outputted towards a SW MGI input. All power detector elements are multiplexed at the input of an amplifier with variable gain that translates the input to the output range 0 – 1.8V. The power detector output is differential, and it can be read either from the ATBP/N pins, or through the ADC. It must be noted that only one detector must be enabled at a time.

The power detector have typically 10dB of dynamic range (frequency flat) when in low power levels (< 0dBm). Its sensitivity can be adjusted for different power levels as shown in Figure 8. This is done by using the digital bits **PDET_GC<5:0>** according to Table 31. In order to power up a specific power detector, enable first the baseband amplifier by setting the bit **PD_PDET_BB** to 0 (default value is 1), and then enable the desired D2P detector by setting the bit **MGIx_PD_D2P_PDET<i>** to 0.

PDET_GC<5:0> ¹ (HEX)	Power range (dBm)
04 ²	[-10, 1]
08	[-13, -2]
10	[-15, -5]
30	[-21, -9]

¹ All residual states are invalid.

² Default value.

Table 31: Power detector range control using PDET_GC bits.

As shown in Figure 21, there are two possible ways to measure the power detector output; either by measuring at the ATBP and ATBN pins, or by using the integrated ADC. The bits **MUX_SEL<1:0>** should be set to 10 in either case. If the ATBP/N pins are used, the **EN_ATB** must be set to 1, and then the ATBP pin will output the positive PDET voltage and the ATBN pin will output the negative PDET voltage. If the ADC is used, the **EN_ATB** must be set to 0, and then proper reading of

the ADC output through SPI is needed.

In order to use a power detector to measure the MGIXx output power, the user has to follow the steps described below:

1. Enable only the MGIX D2P power detector element connected to the PAi, by setting the bit **MGIX_PD_D2P_PDET<i>** = 0. Make sure that all the other power detectors are powered down.
2. Enable the baseband amplifier by setting **PD_PDET_BB** = 0.
3. Select the appropriate level of sensitivity through the bits **PDET_GC<5:0>**, depending on the expected power level.
4. Select the proper input of the auxiliary MUX, by setting **MUX_SEL<1:0>** bits to 10.
5. Use the ATBP/N pins (make sure that **EN_ATB** = 1) or the ADC to measure the detector's value.

The user is advised to calibrate the power detector in case high accuracy is required.

ATB_EN<28:0> ¹	Node to be measured (or switch)	Expected Value (V)
0000 0000 0000 0000 0000 0000 0000 0000	No output. Default value.	
0000 0000 0000 0000 0000 0000 0000 0001	Bandgap voltage	660m
0000 0000 0000 0000 0000 0000 0000 0010	VTMPi Voltage	-
0000 0000 0000 0000 0000 0000 0000 0100	ADC SAR Positive Reference Voltage	0.9
0000 0000 0000 0010 0000 0000 0000 1000	MGIO1 D2P DRV Gm MOS Bias Voltage	0.5
0000 0000 0000 0010 0000 0000 0001 0000	MGIO1 D2P DRV Cascode MOS Bias Voltage	1.8
0000 0000 0000 0010 0000 0000 0010 0000	MGIO1 D2P LDO PA1/2 Output Voltage	1
0000 0000 0000 0010 0000 0000 0100 0000	MGIO1 D2P LDO PA0 Output Voltage	1
0000 0000 0000 0010 0000 0000 1000 0000	MGIO1 D2P PSEL_VGA0 Pos Gm MOS Bias Voltage	0.5
0000 0000 0000 0010 0000 0001 0000 0000	MGIO1 D2P PSEL_VGA0 Pos Casc MOS Bias Voltage	1.2
0000 0000 0000 0010 0000 0010 0000 0000	MGIO1 D2P PSEL_PA0 Lower Bias Voltage	0.5
0000 0000 0000 0010 0000 0100 0000 0000	MGIO1 D2P PSEL_PA0 Upper Bias Voltage	0.625
0000 0000 0000 0010 0000 1000 0000 0000	MGIO1 P2D LDO PS and Mixer driver Output Voltage	1
0000 0000 0000 0010 0001 0000 0000 0000	MGIO1 P2D LDO LNA Output Voltage	1
0000 0000 0000 0010 0010 0000 0000 0000	MGIO1 P2D Active FLT Negative Output Voltage	-
0000 0000 0000 0010 0100 0000 0000 0000	MGIO1 P2D Active FLT Positive Output Voltage	-
0000 0000 0000 0010 1000 0000 0000 0000	MGIO1 P2D Mixer LO Common Mode Voltage	0.45
0000 0000 0000 0011 0000 0000 0000 0000	MGIO1 P2D Active FLT Common Mode Voltage	0.9
0000 0000 0000 0010 0000 0000 0000 0000	MGIO1 ATB Enable	SWITCH
0001 0000 0000 0100 0000 0000 0000 0000	PLL CP Mid Bias Voltage	-
0001 0000 0000 1000 0000 0000 0000 0000	PLL CP nMOS source Bias Voltage	-
0001 0000 0001 0000 0000 0000 0000 0000	PLL CP pMOS source Bias Voltage	-
0001 0000 0010 0000 0000 0000 0000 0000	PLL VCO VREF	1.25
0001 0000 0100 0000 0000 0000 0000 0000	PLL VCO VREF CT	790m
0001 0000 1000 0000 0000 0000 0000 0000	PLL LDO VREF	0.9
0001 0001 0000 0000 0000 0000 0000 0000	PLL LDO OUT MMD	1
0001 0010 0000 0000 0000 0000 0000 0000	PLL LO_DRV VBIAS	0.9
0001 0100 0000 0000 0000 0000 0000 0000	PLL CP VREF	0.5
0001 1000 0000 0000 0000 0000 0000 0000	PLL VTUNE	-
0001 0000 0000 0000 0000 0000 0000 0000	PLL ATB Enable	SWITCH

¹ All residual states are invalid.

Table 32: Analog Test Bus control.

10.3.4 Analog-to-Digital Converter (ADC)

SPIDER APIC 2 is equipped with a 10-bit Successive Approximation Register (SAR) ADC. This ADC is the AKRO_B_AD_111_211_10_TS65G (mentioned as AD111 throughout the document) Akronic IP. It is used to measure one of the following DC signals:

- ATB output
- Power Detector output
- External input, given from ATBP/N pins

These DC signals are given differentially to the ADC input. In order to select the desired signal, the bits **MUX_SEL<1:0>** should be set to 01, 10 and 00 respectively (Table 29).

Programmability

AD111 features a controllable bandwidth at its input signal, adjusted through a low pass filter. This adjustment is configured via the **AD111_BW<1:0>** bits (Table 33). Also the bias current of the block can be controlled through the bits **AD111_BIAS_CC<2:0>** and powered down by the bit **PD_AD111_BIAS** (Table 24), as described in Section 10.3.1.

AD111_BW<1:0>	Bandwidth (MHz)
11	3.54
10	6.2
01	11.5
00 ¹	23

¹Default value.

Table 33: AD111 input bandwidth control.

Other controls are the digital enable, reset and power down of the block, and are described in the following tables. There is also the option for two AD111 signals, the "start" and the "ready", to be measured through the pins ATBN and AD111_READY18, respectively (Tables 28 and 30).

AD111_EN	Operation
0 ¹	AD111 digital circuitry are disabled
1	AD111 digital circuitry are enabled

¹Default value.

Table 34: AD111 digital enable bit settings.

AD111_RST	Operation
0 ¹	Normal mode
1	Reset mode

¹Default value.

Table 35: AD111 reset bit settings.

Note that before asserting the **AD111_EN** signal high, the AD111 must be reset. In order to reset it, a

positive pulse (0→1→0) should be sent to the bit **AD111_RST**.

PD_AD111	Operation
0	AD111 is powered on
1 ¹	AD111 is powered down

¹Default value is 1.

Table 36: AD111 power down bit settings.

Operation

AD111 operational states are described below. The timing diagram for this procedure is shown in Figure 22.

1. Default State:

- Initially, the block is inactive.
- It awaits the activation AD111 "start" (STR) signal, which is controlled by **ADC_READ<0>** bit.
- The block transitions from the default state to the Sampling State when STR goes high.

2. Sampling State:

- Upon detecting a high STR, the block enters the sampling state.
- Sampling begins with the first rising edge of the clock (CLK) signal.
- The SAMPLE signal is generated for the next three clock periods, including the initial one.

3. Comparison State:

- The block advances to the comparison state on the fourth rising edge of CLK.
- During this state, the bits on the DAC bus are set sequentially from MSB to LSB.
- The process of setting each bit continues until the LSB is determined.

4. Ready State:

- The block transitions to the ready state on the following falling edge of CLK after the LSB has been set.
- The AD111 "ready" (READY) signal is asserted high for one clock period, which lasts from this falling edge to the subsequent rising edge of CLK.
- At the midpoint of this state (at the falling edge of CLK), the data bus is loaded with the result.

5. Return to Default State:

- Following the ready state, the block returns to its default state on the next clock cycle.
- The block then remains inactive, waiting for the next STR signal.

Measurement

To perform a measurement using the ADC, a number of steps must be followed to properly configure its operation. As a first step, the user needs to calibrate the ADC to cancel out the unavoidable initial DC offset. To achieve this, the ATBP/N pins can be used as inputs in order to feed a DC signal into the ADC, while the bit **EN_ATB** must be set to 1 and bits **MUX_SEL<1:0>** must be set to 00 (Figure 21).

Furthermore, an SPI clock must be used to implement the necessary sampling frequency. In order for the ADC to work the SPI must continuously be receiving clock

signals. The necessary steps along with the SPI registers that must be configured, are represented in the following list:

1. Select the desired value to measure, either an ATB either a PDET signal. Set **MUX_SEL<1:0>** bits according to Table 29.
2. Set the **EN_ATB** bit to 0, to isolate the ATBP/N pins (Figure 21).
3. Reset the ADC by sending a pulse through the bit **AD111_RST**
4. Enable the ADC by setting the bit **PD_AD111** to 0, as well as the **AD111_EN** bit to 1.
5. If needed, set properly the bits **AD111_STR_SEL** and **EN_AD111_READY18** in order to allow STR and READY signals to pass to the pins ATBN and AD111_READY18, respectively.
6. Send SPI clocks continuously. The ADC is now in the aforementioned default state, waiting for a start signal.

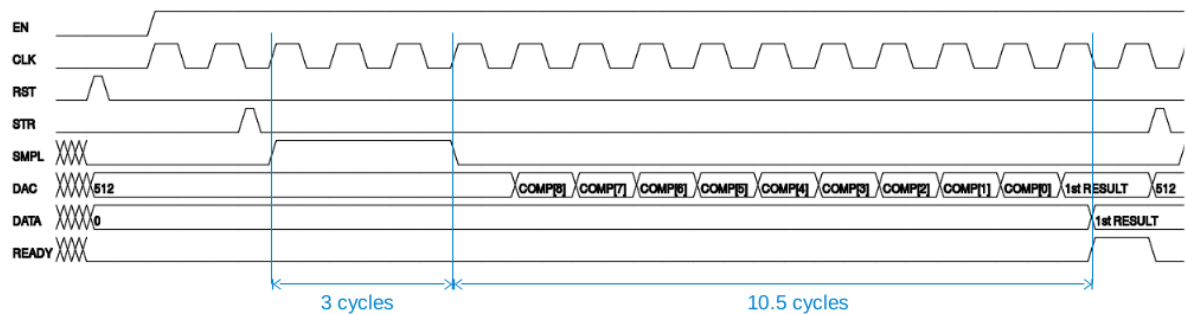


Figure 22: ADC Timing Diagram.

10.4 PLL Digital Controls

The PLL used in *SPIDER APIC 2* is the AKRO_B_PL_312_211_HP_TS65G (mentioned as PL312 throughout the document) Akronic IP. This IP has its standalone datasheet, AKRO_B_PL_310_211_HP_TS65G_Fdatasheet.pdf, which describes in detail all its functionalities and digital controls. In this section the functions and digital controls that are related to the PL312 - MGI interface are explained.

PL312 block diagram is shown in Figure 23. At its output it has the LO Driver (LO_DRV) block, which is able to drive the internally produced LO signal inside and outside the IC, and also to receive an externally produced LO signal as an input. This block offers significant configuration capabilities. Its internal circuitry and digital controls are shown in Figure 24.

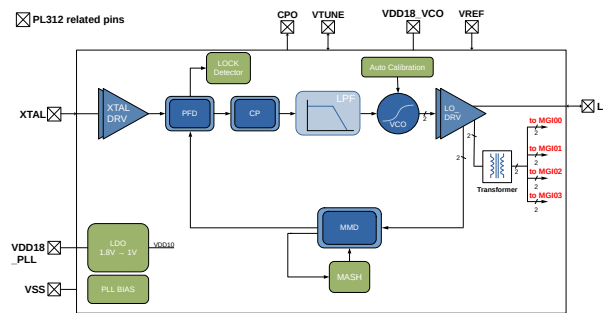


Figure 23: PL312 block diagram.

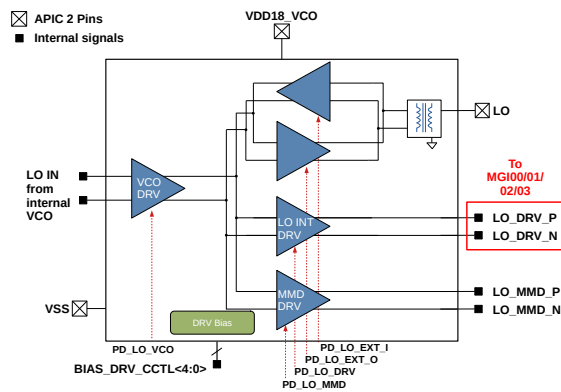


Figure 24: PL312 LO_DRV output driver.

Inside the IC, the LO signal can be propagated to the MMD through the MMD_DRV block, in order to close the PLL loop. It can also be propagated through the LO_INT_DRV block to the MGI blocks, that need an RF reference signal in order to operate. Outside the IC, the signal can be propagated as a single ended output to the LO pin, with an output power that is typically 0dBm, matched on a single ended 50Ω load impedance. There is also the capability to use the LO pin as an input, to get an externally given single-ended LO signal. This input signal is also matched to 50Ω impedance.

From the above it becomes apparent that there are two possible ways to feed the MGIs with an RF signal. For both of them the PL312 LO_DRV has a unique configuration, as shown in Table 37. The first one is to feed the MGIs with an externally generated single-ended RF signal, that will be given as an input through the LO pin and then to the LO_INT_DRV block. This way the PLL loop critical circuitry are not in use, and the PLL is thus bypassed. The frequency of this feed signal can be from 7.5GHz up to 10GHz. The second one is to use the internally produced PLL RF signal and propagate it through the LO_INT_DRV and the MMD_DRV blocks, ignoring the LO pin. The bandwidth of this feed signal can be from 7.9GHz up to 9.8GHz.

LO_DRV Controls // Other characteristics	External MGI RF feed	Internal MGI RF feed
PD_LO_VCO	1	0
PD_LO_DRV	0	0
PD_LO_EXT_O	1	1
PD_LO_EXT_I	0	1
PD_LO_MMD	1	0
PLL input signal	Single-ended RF, from LO pin	Single-ended crystal reference, from XTAL pin
PLL loop	Powered down	Operating
Input signal BW	7.5 - 10GHz	7.9 - 9.8GHz

Table 37: External vs Internal MGI RF feed.

It should be noted that PL310 is generally able to support a frequency ramp generator, a feature especially useful for FMCW RADAR applications. In order to implement the ramp generator an internal memory is necessary. The PL310 used in the *SPIDER APIC 1* is not able to use this feature, since in this sort of an application its advantages can't be found useful enough to justify the inclusion of an internal memory.

11 Serial Peripheral Interface

SPIDER APIC 2 leverages the SPI protocol for its communication needs, equipped with 33 32-bit registers dedicated to the storage of control signals, plus an additional module designed to manage the integrated ADC (AD111). This SPI setup enables two primary operations: the conventional Write and Read, functioning at transmission speeds of up to 250MHz. Uniquely, it allows for the redirection of the AD111 output directly to the SDO18 pin of the IC. In Table 38, the SPI commands and the corresponding operations are being displayed.

Command	Operation
00	Read
01	Write

Table 38: SPI operation command.

The SPI is being reset automatically after power on, but there is also the option to externally reset it, by using the RST18 pin (Table 39). SPI operates normally when the pin is at 0V, and is in reset mode when the pin is at

1.8V. In order to reset it, a 1.8V pulse with minimum width of 1.3ns must be given.

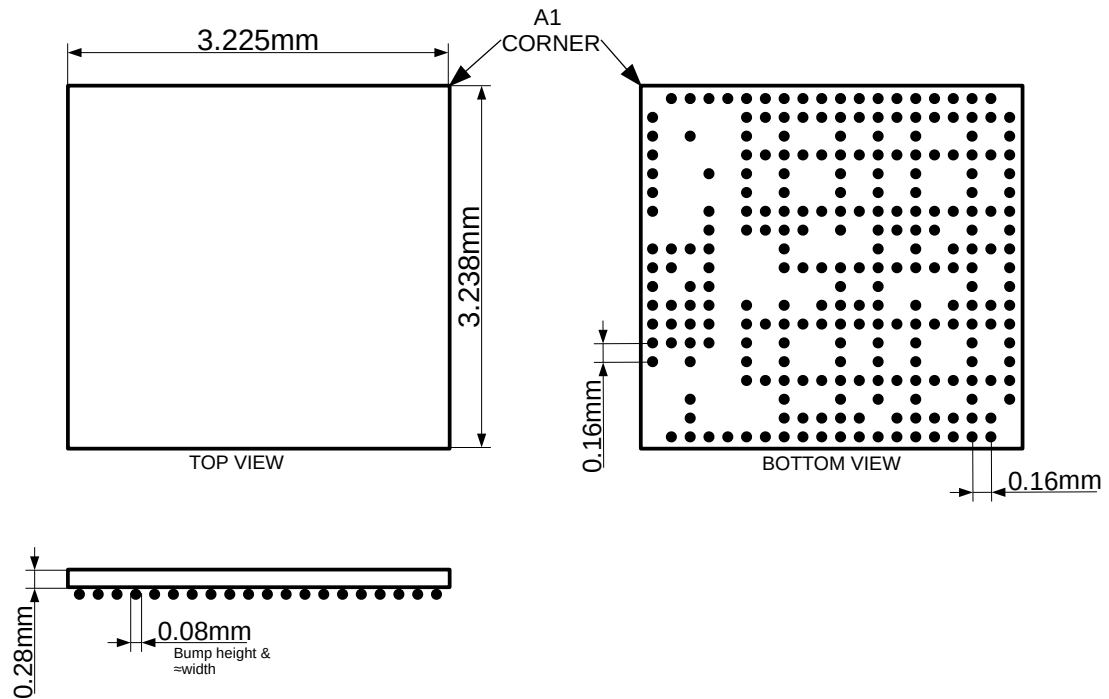
RST18 pin	SPI mode
0V	Normal mode
1.8V	Reset mode

Table 39: SPI external reset.

An array of up to 16 ICs can be controlled via a single 4-wire SPI bus. For the SPI to identify each chip distinctly, a unique 4-bit Chip Address must be assigned to every IC. This assignment is done through configuring the ADR18<3:0> pins externally.

During a Read or Write operation, a 5-bit CHIP_ADDRESS code is required to ensure the correct IC is selected for communication. In this 5-bit code, the 4 least significant bits represent the Chip Address, directly linking to the IC's unique identifier. The MSB, however, is not utilized in the identification process and is thus ignored.

12 Package Outline



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