EUROPEAN COMMISSION

Horizon Europe Framework Programme (HORIZON)
HORIZON-EIC HORIZON EIC Grants
HORIZON Action Grant Budget-Based

GA No. 101070417

Computation Systems Based on Hybrid Spin-wave–CMOS Integrated Architectures

SPIDER - Deliverable report

D6.2 - Report on test chip APIC performance

Disclaimer/ Acknowledgment

Funded by the European Union (under grant agreement No. 101070417).

About SPIDER

In the future, the miniaturisation of electronic devices– epitomised by Moore's law – will be progressively limited by increasing power densities and the associated chip heating. Moreover, autonomous microelectronic applications, for example for the Internet of Things, demand high performance at ultra-low power. Therefore, much research has recently focused on disruptive computing technologies that limit power consumption and optimise performance per circuit area. Spin wave computing is a disruptive spintronic technology that uses the interference of spin waves for computation and has considerable potential for power and area reduction per computing throughput. Despite much recent progress in the realisation of spin wave logic gates, no concept for a complete computing system exists today that is based only on spin waves. Thus, to advance from devices to systems, spin wave devices need to be complemented by CMOS in a hybrid spin wave–CMOS system. Using an interdisciplinary approach joining partners with expertise in materials science, physics, device manufacturing, electrical engineering, circuit design, and packaging, SPIDER targets the demonstration of a complete operational hybrid spin wave–CMOS computing system. To date, complex spin wave circuits are yet to be realised. SPIDER targets to fill this gap by developing spin wave logic circuits based on majority gates. To embed these circuits into a CMOS environment, SPIDER will design mixed signal CMOS chips that can drive spin wave circuits and read out computation results. The spin wave and CMOS chips will then be combined on an interposer to obtain the final hybrid system. This work will pave the way towards viable spin wave chips and provide a first benchmark of spin wave computing at the system level. Based on the results, SPIDER will then develop a roadmap to advance spin wave technology to compete with CMOS in technology nodes below 1 nm.

SPIDER consortium members

Document information

Deliverable No.	D6.2
Related WP	WP6
Deliverable Title	Report on test chip APIC performance
Deliverable Date	28 – February - 2025
Deliverable Type	Report
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Document history

Date	Revision	Prepared by	Approved by	Description
20/Nov/2024	1	Panagiotis Kassanos	Nikos Naskas	First draft
05/02/2025	2	Panagiotis Kassanos	Nikos Naskas	Second draft
21/02/2025	3	Panagiotis Kassanos	Nikos Naskas	Final version

Dissemination level

PU	**Public**	
SEN	**Sensitive**	x

Publishable summary

Deliverable D6.2 focuses on the experimental characterization of APIC-1 through the use of evaluation board EVB-1. Originally planned as a simple IC with test structures, APIC-1 was developed as a complete and stand-alone IC, in order to facilitate early in the project the experimental verification of all required circuit blocks and to demonstrate hybrid system implementation. This approach enables issues to be identified early in the project, to be ratified through the second tape-out and to thus ensure project success. APIC-1 thus was implemented to have various features not needed for the final APIC implementation and the adder realization, that allowed the full system characterization and minimized the impact of potential issues in this effort. EVB-1 has been developed to allow characterization of two MGIs. One connected to an on-chip PLL and one independent of the PLL. A GUI was developed to control the EVB/APIC and facilitate the testing process. In addition, various routines were written to control the various laboratory instruments required and to allow the automatic testing of APIC-1 and the collection and plotting of all results. This is particularly important, as it allows the characterization of several boards by speeding up the testing process significantly. Testing of several IC's enables the statistical analysis of the performance of the IC, which is particularly important in this project, as several IC will be used to create the project's final demonstrator, a full adder comprised of eight ICs. The de-embedding board created was first used to characterize the RF paths on the EVB for calibration purposes. These measurements were used to compensate for the losses on the board and to assess the actual performance of APIC-1. This report presents the characterization results obtained through the above. Overall, the characterization of APIC-1 was successful, with the IC behaving as expected from simulations.