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Computation Systems Based on Hybrid Spin-wave–CMOS Integrated Architectures

SPIDER - Deliverable report

D3.3 - Final APIC tape-out

Disclaimer/ Acknowledgment

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About SPIDER

In the future, the miniaturisation of electronic devices– epitomised by Moore's law – will be progressively limited by increasing power densities and the associated chip heating. Moreover, autonomous microelectronic applications, for example for the Internet of Things, demand high performance at ultra-low power. Therefore, much research has recently focused on disruptive computing technologies that limit power consumption and optimise performance per circuit area. Spin wave computing is a disruptive spintronic technology that uses the interference of spin waves for computation and has considerable potential for power and area reduction per computing throughput. Despite much recent progress in the realisation of spin wave logic gates, no concept for a complete computing system exists today that is based only on spin waves. Thus, to advance from devices to systems, spin wave devices need to be complemented by CMOS in a hybrid spin wave–CMOS system. Using an interdisciplinary approach joining partners with expertise in materials science, physics, device manufacturing, electrical engineering, circuit design, and packaging, SPIDER targets the demonstration of a complete operational hybrid spin wave–CMOS computing system. To date, complex spin wave circuits are yet to be realised. SPIDER targets to fill this gap by developing spin wave logic circuits based on majority gates. To embed these circuits into a CMOS environment, SPIDER will design mixed signal CMOS chips that can drive spin wave circuits and read out computation results. The spin wave and CMOS chips will then be combined on an interposer to obtain the final hybrid system. This work will pave the way towards viable spin wave chips and provide a first benchmark of spin wave computing at the system level. Based on the results, SPIDER will then develop a roadmap to advance spin wave technology to compete with CMOS in technology nodes below 1 nm.

SPIDER consortium members

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Lead Author	Panagiotis Kassanos (Akronic P.C.)
Co-Author(s)	Ilias Tsakiridis (Akronic P.C.), Dimitris Kalampakas (Akronic P.C.), Nikolaos Naskas (Akronic P.C.).

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Publishable summary

Deliverable D3.3 focuses on the final tape-out of the SPIDER analogue periphery integrated circuit (APIC). This second APIC follows the same overall concept of the first tape-out. The main differences are the re-tuning of the PLL to cover a range of lower frequencies (5.92 - 6.9 GHz), which also necessitated the re-tuning of the PLL input and output baluns. Additional changes include a change in the power amplifiers of the D2P block driving each MAJ gate antenna to include a tuning circuit (LC tank) to make the D2P bandpass (4.5-7.5 GHz) and reduce the overall power consumption by about 5 mA and a reduction to the phase shifter's inverter size to reduce the current consumption to 4 mA from 10 mA. At an overall system architecture level, the option to use an external differential signal source has been removed and all MGI's are stimulated through the PLL, either through a signal generated by the PLL, or one provided externally to the PLL output driver. This necessitated the use of a common feeding network for all four MGIs. Thus, the various building blocks were rearranged on the die, leading to a new pin-out for the APIC. A final change to note is the addition of the signals controlling the excitation phase of the D2P and the readout of the P2D to the SPI, such that they can be controlled or read through a PC.