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Computation Systems Based on Hybrid Spin-wave–CMOS Integrated Architectures

SPIDER - Deliverable report

D3.2- Evaluation Board for Test Structure APIC

Disclaimer/ Acknowledgment

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About SPIDER

In the future, the miniaturisation of electronic devices– epitomised by Moore's law – will be progressively limited by increasing power densities and the associated chip heating. Moreover, autonomous microelectronic applications, for example for the Internet of Things, demand high performance at ultralow power. Therefore, much research has recently focused on disruptive computing technologies that limit power consumption and optimise performance per circuit area. Spin wave computing is a disruptive spintronic technology that uses the interference of spin waves for computation and has considerable potential for power and area reduction per computing throughput. Despite much recent progress in the realisation of spin wave logic gates, no concept for a complete computing system exists today that is based only on spin waves. Thus, to advance from devices to systems, spin wave devices need to be complemented by CMOS in a hybrid spin wave–CMOS system. Using an interdisciplinary approach joining partners with expertise in materials science, physics, device manufacturing, electrical engineering, circuit design, and packaging, SPIDER targets the demonstration of a complete operational hybrid spin wave–CMOS computing system. To date, complex spin wave circuits are yet to be realised. SPIDER targets to fill this gap by developing spin wave logic circuits based on majority gates. To embed these circuits into a CMOS environment, SPIDER will design mixed signal CMOS chips that can drive spin wave circuits and read out computation results. The spin wave and CMOS chips will then be combined on an interposer to obtain the final hybrid system. This work will pave the way towards viable spin wave chips and provide a first benchmark of spin wave computing at the system level. Based on the results, SPIDER will then develop a roadmap to advance spin wave technology to compete with CMOS in technology nodes below 1 nm.

SPIDER consortium members

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Publishable summary

Deliverable D3.2 focuses on the development of the SPIDER evaluation board (EVB-1) of the analogue periphery integrated circuit (APIC-1). The motivation for the development of the EVB lies on the requirement for the characterization of all the functional blocks of the APIC and overall operation of each block interfacing with the spin wave magnonic majority gates (MAJ). The board has an SPI controller, allowing control of the APIC through a PC and a graphical user interface (GUI). The APIC has four majority gate interface circuits (MGI) that are split into two groups depending on whether they are interfaced with the APIC's phase-locked loop (PLL). Through SMA connectors, the input RF excitation signals for the digital to phase (D2P) sub-blocks of these two MGIs can be applied to the APIC and the resulting output excitation signals to the MAJ gate can be measured. The phase of each signal can be set either though headers or through the SPI controller and a PC. SMA connectors can also be used to apply RF signals to the inputs of the phase to digital (P2D) readout circuits. The computational output of the readout channels can be read through header or through the SPI controller and a PC. The PLL and ADC of the APIC can also be fully characterized, and the APIC's analog test bus (ATB) can also be used to measure various internal nodes. The RF transitions from the APIC towards the lower layers of the board where the MAJ gates will sit were simulated and the board was manufactured according to the design rules of the state-of-the-art process developed by Fraunhofer IZM. The multilayer board consists of six layers of ~35 µm thick ABF with a ~550 µm thick core with eight layers of Cu. Only three Cu layers sitting on the top three ABF layers are used for the circuit and the remaining structure serves the purpose of achieving a symmetrical and thus mechanically robust structure. The core layer is where the SW chip will sit. This board will also be used for the first hybrid demonstrator, which will use the two MGIs not being interfaced with the SMA connectors. In addition to testing the, APIC, the purpose of this board is thus also to ensure design, simulation, packaging, manufacturing and assembly requirements and specifications are aligned and that potential issues are identified and solved early in the project.