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Computation Systems Based on Hybrid Spin-wave–CMOS Integrated Architectures

SPIDER – Interim Project Report

D1.2 - Interim Project Report

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About SPIDER

In the future, the miniaturisation of electronic devices– epitomised by Moore's law – will be progressively limited by increasing power densities and the associated chip heating. Moreover, autonomous microelectronic applications, for example for the Internet of Things, demand high performance at ultralow power. Therefore, much research has recently focused on disruptive computing technologies that limit power consumption and optimise performance per circuit area. Spin wave computing is a disruptive spintronic technology that uses the interference of spin waves for computation and has considerable potential for power and area reduction per computing throughput. Despite much recent progress in the realisation of spin wave logic gates, no concept for a complete computing system exists today that is based only on spin waves. Thus, to advance from devices to systems, spin wave devices need to be complemented by CMOS in a hybrid spin wave–CMOS system. Using an interdisciplinary approach joining partners with expertise in materials science, physics, device manufacturing, electrical engineering, circuit design, and packaging, SPIDER targets the demonstration of a complete operational hybrid spin wave–CMOS computing system. To date, complex spin wave circuits are yet to be realised. SPIDER targets to fill this gap by developing spin wave logic circuits based on majority gates. To embed these circuits into a CMOS environment, SPIDER will design mixed signal CMOS chips that can drive spin wave circuits and read out computation results. The spin wave and CMOS chips will then be combined on an interposer to obtain the final hybrid system. This work will pave the way towards viable spin wave chips and provide a first benchmark of spin wave computing at the system level. Based on the results, SPIDER will then develop a roadmap to advance spin wave technology to compete with CMOS in technology nodes below 1 nm.

SPIDER consortium members

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Publishable summary

This report contains a summary of the progress of SPIDER during the first 12 months, to be reviewed at the first technical interim meeting. After an executive summary of the work and the current status of SPIDER, the work carried out is discussed on a technical level organized per work package.

The initial activities of SPIDER during the first 12 months focused on the development of the basic concepts of the hybrid spin-wave-CMOS system. Ater the basic principles for the system-technology co-design had been established, concepts and designs were developed for the three parts of the final system: the spin-wave chip, the CMOS APIC, and the interposer.

In a first step in the development of the spin-wave chip, SPIDER selected YIG as the base material because of its low damping, long attenuation lengths, and the resulting flexibility in device design. Spin-wave majority gates were designed using U-shaped microwave antennas as transducers and a lithography mask for a test chip is now available. The development of unit process steps for spin-wave device manufacturing has been finalized and first devices are currently being processed.

In parallel, SPIDER has developed a driver concept for a spin-wave majority gate. This has allowed for the design of a first APIC test ship, which will allow to drive single majority gates using digital input signals. Presently, final design efforts are ongoing.

Spin-wave and APIC chips will be packaged using an interposer based on PCB technology. A first interposer design is currently finalized, including for evaluation boards for APIC and spin-wave chip. This will enable the fabrication of first packaged spin-wave chips in the near future.

The activities of SPIDER aim at the fabrication and characterization of a first hybrid test system with the possibility to drive single spin-wave majority gates from digital signals at the end of 2024. The resulting learning will then allow SPIDER to advance forwards a system incorporating a complex spin-wave circuit, such as an adder. A roadmap will be developed at the end of SPIDER to probe pathways to hybrid systems that can outperform CMOS for specific applications.