EUROPEAN COMMISSION

Horizon Europe Framework Programme (HORIZON)
HORIZON-EIC HORIZON EIC Grants
HORIZON Action Grant Budget-Based

GA No. 101070417

Computation Systems Based on Hybrid Spin-wave–CMOS Integrated Architectures

SPIDER - Deliverable report

D3.1- Test structure APIC tape-out

Disclaimer/ Acknowledgment

Funded by the European Union (under grant agreement No. 101070417).

About SPIDER

In the future, the miniaturisation of electronic devices– epitomised by Moore's law – will be progressively limited by increasing power densities and the associated chip heating. Moreover, autonomous microelectronic applications, for example for the Internet of Things, demand high performance at ultra-low power. Therefore, much research has recently focused on disruptive computing technologies that limit power consumption and optimise performance per circuit area. Spin wave computing is a disruptive spintronic technology that uses the interference of spin waves for computation and has considerable potential for power and area reduction per computing throughput. Despite much recent progress in the realisation of spin wave logic gates, no concept for a complete computing system exists today that is based only on spin waves. Thus, to advance from devices to systems, spin wave devices need to be complemented by CMOS in a hybrid spin wave–CMOS system. Using an interdisciplinary approach joining partners with expertise in materials science, physics, device manufacturing, electrical engineering, circuit design, and packaging, SPIDER targets the demonstration of a complete operational hybrid spin wave–CMOS computing system. To date, complex spin wave circuits are yet to be realised. SPIDER targets to fill this gap by developing spin wave logic circuits based on majority gates. To embed these circuits into a CMOS environment, SPIDER will design mixed signal CMOS chips that can drive spin wave circuits and read out computation results. The spin wave and CMOS chips will then be combined on an interposer to obtain the final hybrid system. This work will pave the way towards viable spin wave chips and provide a first benchmark of spin wave computing at the system level. Based on the results, SPIDER will then develop a roadmap to advance spin wave technology to compete with CMOS in technology nodes below 1 nm.

SPIDER consortium members

imec THALES

TU Delft Delft University of Technology

Fraunhofer IZM

RPTU IMT Akronic

Document information

Deliverable No.	D3.1
Related WP	WP3
Deliverable Title	Test structure APIC tape-out
Deliverable Date	30 – November - 2023
Deliverable Type	Report
Lead Author	Panagiotis Kassanos (Akronic P.C.)
Co-Author(s)	Ilias Tsakiridis (Akronic P.C.), Ioannis Kousparis (Akronic P.C.), Dimitris Kalampakas (Akronic P.C.), Nikolaos Alexiou (Akronic P.C.), Nikolaos Naskas (Akronic P.C.).

Document history

Date	Revision	Prepared by	Approved by	Description
30/Nov/2023	1	Panagiotis Kassanos	Nikos Naskas	First draft
12/Jan/2024	2	WP Leader	Nikos Naskas, Christoph Adelmann	Final version

Dissemination level

PU	**Public**	
SEN	**Sensitive**	X

Publishable summary

Deliverable D3.1 focuses on the development of the SPIDER analogue periphery integrated circuit (APIC). The motivation for the development of the APIC lies on the fact that with the current state of the art, it is not yet possible to create an all-magnonic circuit, due to challenges currently faced related with the weak output signal of each gate. It is thus not possible to cascade logic gates. In addition, there has not been any other integrated circuit implementation with the SPIDER APIC capabilities dedicated for magnonic MAJ gate arrays and a magnonic MAJ gate-based full adder has never before been realized. The APIC is responsible for generating the appropriate excitation signals for each of the three inputs of a magnonic majority (MAJ) gate. These signals are generated from a single common reference signal that is either externally provided or via an on-chip phase-locked loop (PLL). Logic levels are encoded in the phase of the signal. A logical 0 is a 0o phase signal and a logical 1 is an 180o out of phase signal. A low frequency signal for each MAJ gate input that is provided externally to the APIC dictates whether a 1 or a 0 is applied to each of the three inputs. The resulting MAJ gate output signal is recorded by the APIC and is compared with the global reference signal. A phase shifter (PS) can be used to compensate phase delays imposed to the signal as it travels from the APIC outputs to the MAJ gate and back to the APIC through the interposer, to reduce computational errors. The comparison through synchronous demodulation leads to a DC signal carrying the information. This and its inverse are led to APIC pads and can be used to control the excitation inputs of other MAJ gates, through the interposer, thus allowing the realization of circuits composed by more than one MAJ gate. The APIC also has all the necessary biasing circuits, including low drop-out voltage regulators, bandgap current references, a serial peripheral interface (SPI) for communication and control, a chip address to allow several chips being controlled through the same SPI bus, and of course low noise amplifiers (LNA), mixers, transimpedance amplifiers (TIA) and other circuits required to implement the various APIC functionalities.