EUROPEAN COMMISSION

Horizon Europe Framework Programme (HORIZON)
HORIZON-EIC HORIZON EIC Grants
HORIZON Action Grant Budget-Based

GA No. 101070417

Computation Systems Based on Hybrid Spin-wave–CMOS Integrated Architectures

SPIDER - Deliverable report

D2.1 - Cascaded SW MAJ3 device design and optimization

Disclaimer/ Acknowledgment

Funded by the European Union (under grant agreement No. 101070417).

About SPIDER

In the future, the miniaturisation of electronic devices– epitomised by Moore's law – will be progressively limited by increasing power densities and the associated chip heating. Moreover, autonomous microelectronic applications, for example for the Internet of Things, demand high performance at ultralow power. Therefore, much research has recently focused on disruptive computing technologies that limit power consumption and optimise performance per circuit area. Spin wave computing is a disruptive spintronic technology that uses the interference of spin waves for computation and has considerable potential for power and area reduction per computing throughput. Despite much recent progress in the realisation of spin wave logic gates, no concept for a complete computing system exists today that is based only on spin waves. Thus, to advance from devices to systems, spin wave devices need to be complemented by CMOS in a hybrid spin wave–CMOS system. Using an interdisciplinary approach joining partners with expertise in materials science, physics, device manufacturing, electrical engineering, circuit design, and packaging, SPIDER targets the demonstration of a complete operational hybrid spin wave–CMOS computing system. To date, complex spin wave circuits are yet to be realised. SPIDER targets to fill this gap by developing spin wave logic circuits based on majority gates. To embed these circuits into a CMOS environment, SPIDER will design mixed signal CMOS chips that can drive spin wave circuits and read out computation results. The spin wave and CMOS chips will then be combined on an interposer to obtain the final hybrid system. This work will pave the way towards viable spin wave chips and provide a first benchmark of spin wave computing at the system level. Based on the results, SPIDER will then develop a roadmap to advance spin wave technology to compete with CMOS in technology nodes below 1 nm.

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Document information

Deliverable No.	D2.1
Related WP	WP2
Deliverable Title	Cascaded SW MAJ3 device design and optimization
Deliverable Date	20 – December - 2023
Deliverable Type	Report
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Document history

Date	Revision	Prepared by	Approved by	Description
05/12/2023	1	Task Leader	WP Leader	First draft
19/12/2023	2	Task Leader	WP Leader	Second draft
31/12/2023	3	WP Leader	Coordinator	Final

Dissemination level

PU	**Public**	
SEN	**Sensitive**	x

Publishable Summary

While there are various ways to let Spin Waves (SWs) carry and process information, the most natural approach is to encode information within their phases. As such, given a certain reference, Boolean values 0 and 1 can be conveyed by same amplitude SWs with a phase shift of 0 and π, respectively. By their very nature, when present into the same waveguide, an odd number of such SWs interact constructively (if in phase) and destructively (if out of phase), providing a natural support for the Majority function evaluation. Up to date, various three input majority (MAJ3) gates have been proposed and validated experimentally or by means of micromagnetic simulation. Given that MAJ3 and Inverter, (signal inversion is obtained by properly adjusting the gate output position) constitute a universal Gate Set one could assume that that the avenue form gates to circuits is wide open. Unfortunately, connecting MAJ3 gates to form larger circuits within the SW domain is not straightforward. Due to their very operation principle, SW MAJ gates are not input/output coherent. While, for proper operation, the gate inputs should be unit amplitude SWs the gate output strength is input data dependent and can assume unit value in case of a weak majority (2 inputs are 0/1 the other is 1/0) and about 3 times the unite value for strong majority (all inputs are the same). Such a strong SW output cannot be directly utilized as input for a follow-up MAJ3 gate as it violates the equality of votes assumption and makes it malfunction. This precludes the direct utilization of a MAJ3 output as input for a follow up gate and place a big hurdle on the road towards SW circuits.

The straightforward solution for building larger MAJ3 based circuits is achieve signal normalization by means of SW to charge and back domain conversion after every gate in the circuit. While this can be achieved by means of Complementary Metal-Oxide Semiconductor (CMOS) implemented repeaters/converters able to normalize the signal before passing it as input to another MAJ3 gate, this is a power-hungry solution, which could potentially nullify the ultra-low power promise of the SW based computation. In view of this, we investigated domain conversion free power effective MAJ3 gate cascading methods able to normalize 'strong' signals while not affecting the 'weak' ones.

In this deliverable we introduce and analyse three methods to normalize the MAJ3 gate output such that it can be directly utilized as input for a follow-up MAJ3 gate. In Section 2.2 we review the possibility to make used of a lateral coupler as a normalizer for 'strong' signal outputs. Further, we build on this, and consider a vertical coupler geometry in Section 2.3 to improve its performance and make it a more effective normalization device. Unfortunately, while coupler-based approaches provide certain advantages, none of them seems to be appropriate for the realization of the target SPIDER circuit demonstrators. For this reason, in Section 2.4 we propose the design of a more powerful logical gate that is basically built by the direct connection of two MAJ3 gates. This approach doesn't rely on any normalization attempt, but it naturally deals with the 'weak' and 'strong' majority situation by taking advantage of SW amplitude decay induced by propagation within the gate waveguide. After demonstrating the 2 MAJ3 gate structure proper behavior by means of micromagnetic simulations we analyze the implication of its utilization for the implementation of an 8-bit Brent Kung adder, which results into 50% reduction in the number of conversions between domains, thus in significant power consumption reduction. Our analysis indicates that such an approach can pave the way towards the potential realization of hybrid ultra-low power SW-CMOS circuits, and we plan to focus a significant part of our future research efforts on the extension, optimization, and the detailed design of 2 MAJ3 gate structures that can properly operate under SPIDER technological limitations and can be utilized in conjunction with normal MAJ3 gates for the implementation of the hybrid 8-bit Brent Kung adder.

Contents

List of acronyms, abbreviations and definitions

Abbreviation	Definitions
SW(-s)	Spin Wave(-s)
MAJ3	Three inputs majority gate
CMOS	Complementary Metal-Oxide Semiconductor
BVSW(-s)	Backward Volume Spin Wave(-s)
SSW(-s)	Surface Spin Wave(-s)
FVSW(-s)	Forward Volume Spin Wave(-s)

1. Introduction

Over the last few years, a lot of advancements have been reported within the magnonics field [1], which are encouraging the belief that magnonic circuits will eventually replace Complementary Metal-Oxide Semiconductor (CMOS) counterparts [2], [3]. One obstacle however that persists since the beginning of the field is the difficulty of manipulating signals in such magnonic circuits. CMOS based circuits have the flexibility that current propagates through wires and such wires can be connected in any possible way. Magnonic circuits on the other hand depend on the utilization of magnetic materials, which aren't so friendly when it comes to constructing or connecting different geometries. Apart from this, the majority gates (MAJ) [4]–[9] which are the main Spin Waves (SWs) computing basic building blocks, rely on the interference between three or more, always an odd, number of spin waves. This interference can be either constructive or destructive based on the phase difference between the waves and a reference signal. However, depending on the input values the result of such interference can result either in a 'weak' or a 'strong' majority output. The 'weak' majority is a SW with the same amplitude as the gate input waves, so it doesn't really create a problem in circuit design, but the 'strong' majority is the result of the constructive interference between three same phase spin waves and thus results in a signal with an amplitude about three times greater than that of the input wave. Due to this input data dependent gate output strengths fan-out or gate cascading within the SW domain cannot be directly achieved. This problem can be dealt with by performing SW to charge and back domain conversions, but this is quite expensive in terms of power consumption and may result in nullifying the ultra-low paper potential of SW based information processing. In this deliverable we present our findings in relation with signal normalization by means of: (i) controlled SW energy exchange between closely coupled waveguides placed in lateral or vertical proximity and (ii) introduce a two majority gates cascading scheme that take advantage of SW degradation to achieve signal normalization. In summary, in this deliverable we introduce three approaches to tackle fan-out and cascading issues within magnonics circuits and discuss their corresponding advantages and disadvantages. The three approaches are:

- **Lateral Coupler**
- **Vertical Coupler**
- **Cascaded Majority Gate**

Note that this deliverable is part Work Package 2 (WP2), which focuses on the spin wave circuit design and optimization to maximize its efficiency. WP2 package aims to pave the way into the design and realization of SW-based circuits and simplify this process so that real life logic circuit can be efficiently implemented in the SW domain. The completion of this work package is meant to offer many possibilities for the design of spin wave-based circuits and to establish the field as a serious contender to current technologies.

WP2 encompasses three tasks that aim to accomplish for its impacts to be long lasting and boost the development of the field as follows:

- **Design of test SW structures**
- **Desing of n-bit Brent-Kung adders**
- **Benchmark and roadmap**

Specifically, this deliverable focuses on the first mentioned task which aims to develop spin wave-based test structures. These structures serve as example designs to study the spin waves behaviour and properties in different designs and reach some conclusions related to required approach for designing more complex SW circuits. An important aspect related to complex SW circuit design is gate cascading problem or the direct connection of logic gates in the SW domain, which is further discussed in this deliverable.