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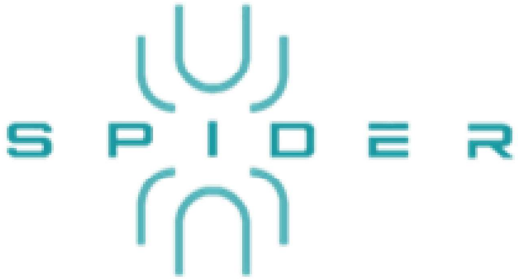
Computation Systems Based on Hybrid Spin-wave–CMOS Integrated Architectures



SPIDER - Deliverable report

D5.1- Initial STCD document

Disclaimer/ Acknowledgment

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About SPIDER

In the future, the miniaturisation of electronic devices– epitomised by Moore's law – will be progressively limited by increasing power densities and the associated chip heating. Moreover, autonomous microelectronic applications, for example for the Internet of Things, demand high performance at ultralow power. Therefore, much research has recently focused on disruptive computing technologies that limit power consumption and optimise performance per circuit area. Spin wave computing is a disruptive spintronic technology that uses the interference of spin waves for computation and has considerable potential for power and area reduction per computing throughput. Despite much recent progress in the realisation of spin wave logic gates, no concept for a complete computing system exists today that is based only on spin waves. Thus, to advance from devices to systems, spin wave devices need to be complemented by CMOS in a hybrid spin wave–CMOS system. Using an interdisciplinary approach joining partners with expertise in materials science, physics, device manufacturing, electrical engineering, circuit design, and packaging, SPIDER targets the demonstration of a complete operational hybrid spin wave–CMOS computing system. To date, complex spin wave circuits are yet to be realised. SPIDER targets to fill this gap by developing spin wave logic circuits based on majority gates. To embed these circuits into a CMOS environment, SPIDER will design mixed signal CMOS chips that can drive spin wave circuits and read out computation results. The spin wave and CMOS chips will then be combined on an interposer to obtain the final hybrid system. This work will pave the way towards viable spin wave chips and provide a first benchmark of spin wave computing at the system level. Based on the results, SPIDER will then develop a roadmap to advance spin wave technology to compete with CMOS in technology nodes below 1 nm.

SPIDER consortium members

imec THALES TU Delft Delft University of Technology Fraunhofer IZM RPTU IMT Akronic

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25/May/2023	2	WP Leader	Coordinator	Deliverable State

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PU	**Public**	
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Publishable summary

The intention of this document is to record all the technical conditions, parameters and important details that were agreed upon in the joint technical consultations. The document should serve as a reference for the processing of the project, since already agreed aspects can be looked up here. In this respect, the STCD can be described as a "living" document, which will be further developed over the course of the project and will ultimately contain the final description of the scientific and technical implementation of the SPIDER project. The STCD takes on the character of a deliverable at this point, however, since all the tuning (including estimation, calculation and smaller preliminary tests) has now been completed and incorporated into the current status, and the project can now move on to test setups for subsystems of the later demonstrator. In this sense, the first version of the STCD, which enables SPIDER hardware setups, is now available with the deliverable. The input of the STCD comes from WP2 to 4. This deliverable also leads directly to hardware setups, which are then presented in publications with a focus on their technical features.