

EUROPEAN COMMISSION

Horizon Europe Framework Programme (HORIZON)

HORIZON-EIC HORIZON EIC Grants

HORIZON Action Grant Budget-Based

GA No. 101070417

Computation Systems Based on Hybrid Spin-wave–CMOS Integrated Architectures



SPIDER - Deliverable report

D1.1- Data management plan and project handbook

Disclaimer/Acknowledgment



Funded by the
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Funded by the European Union (under grant agreement No. 101070417).

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About SPIDER

In the future, the miniaturisation of electronic devices— epitomised by Moore’s law – will be progressively limited by increasing power densities and the associated chip heating. Moreover, autonomous microelectronic applications, for example for the Internet of Things, demand high performance at ultralow power. Therefore, much research has recently focused on disruptive computing technologies that limit power consumption and optimise performance per circuit area. Spin wave computing is a disruptive spintronic technology that uses the interference of spin waves for computation and has considerable potential for power and area reduction per computing throughput. Despite much recent progress in the realisation of spin wave logic gates, no concept for a complete computing system exists today that is based only on spin waves. Thus, to advance from devices to systems, spin wave devices need to be complemented by CMOS in a hybrid spin wave–CMOS system. Using an interdisciplinary approach joining partners with expertise in materials science, physics, device manufacturing, electrical engineering, circuit design, and packaging, SPIDER targets the demonstration of a complete operational hybrid spin wave–CMOS computing system. To date, complex spin wave circuits are yet to be realised. SPIDER targets to fill this gap by developing spin wave logic circuits based on majority gates. To embed these circuits into a CMOS environment, SPIDER will design mixed signal CMOS chips that can drive spin wave circuits and read out computation results. The spin wave and CMOS chips will then be combined on an interposer to obtain the final hybrid system. This work will pave the way towards viable spin wave chips and provide a first benchmark of spin wave computing at the system level. Based on the results, SPIDER will then develop a roadmap to advance spin wave technology to compete with CMOS in technology nodes below 1 nm.

SPIDER consortium members



Document information

Deliverable No.	D1.1
Related WP	WP1
Deliverable Title	Data management plan and project handbook
Deliverable Date	31 - 05 - 2023
Deliverable Type	Report
Lead Author	Christoph Adelman (IMEC), Xia Han (IMEC)
Co-Author(s)	Florin Ciubotaru (IMEC), Martin Hempel (FRAUNHOFER), Paolo Bortolotti (THALES), Philipp Pirro (RPTU), Moritz Geilen (RPTU), Alina Bunea (IMT), Pantazis Anagnostou (TUD), Panagiotis Kassanos (AKRONIC)

Document history

Date	Revision	Prepared by	Reviewed by	Description
10/05/2023	1	Xia Han	Christoph Adelman	First draft
01/06/2023r	2	WP Leaders	Christoph Adelman	Final

Dissemination level

PU	Public	
SEN	Sensitive	x

Publishable summary

This deliverable is an internal deliverable describing:

- the detailed data management plan, with input from all partners. This part describes the types of data generated by the project, how they are handled and stored, as well as measures to optimize data reuse. Published data can be shared with outside researchers following standard academic practices upon reasonable request. Unpublished data cannot be shared for IP reasons.
- the project handbook with a Gantt chart and a Work Breakdown Structure (WBS), including a schedule per task, responsible partner, related subtasks, related deliverables, and dependencies with respect to other tasks.